NNCI Annual Meeting

27 October 2023

Trevor Thornton (Arizona State University),
Shyam Aravamudhan (North Carolina A&T State University),
Mary Tang (Stanford),
Sanjay Banerjee (UT Austin),
Philip Wong (Stanford)

Microelectronics/Semiconductors Research Community

Virtual workshop held in September 2022

Microelectronics/ Semiconductor Research Community Virtual Workshop

September 8 and 9, 2022 12pm – 3:30 pm EDT

Hosted by NSF National Nanotechnology Coordinated Infrastructure (NNCI) Program

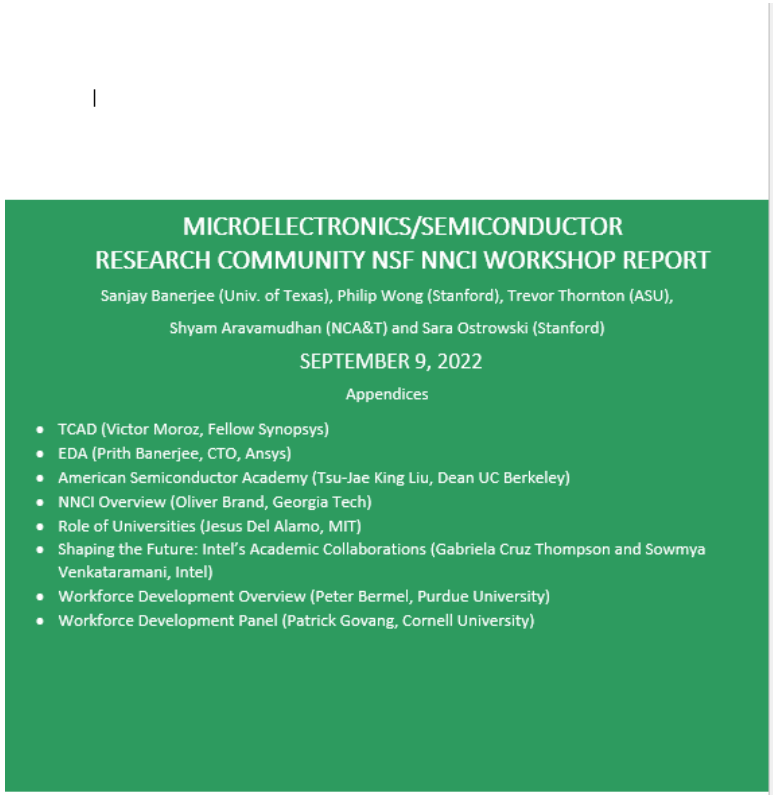
Organizers: Philip Wong (Stanford), Trevor Thornton (Arizona State), Shyam Aravamudhan (North Carolina A&T Univ.) and Sanjay Banerjee (Univ. of Texas)

"The anticipated outcome of this workshop will be developing a report that could inform CHIPS funding as it relates to USICA, NSTC, NAMP and the Microelectronics Commons, as well as NSF Engines and FuSe".

National Nanotechnology Coordinated Infrastructure NCI Southwest TNF RTNN nano@stanford

Microelectronics/Semiconductors Research Community

Report published December 2022



MICROELECTRONICS/SEMICONDUCTOR
RESEARCH COMMUNITY NSF NNCI WORKSHOP REPORT

Sanjay Banerjee (Univ. of Texas), Philip Wong (Stanford), Trevor Thornton (ASU),

Shyam Aravamudhan (NCA&T) and Sara Ostrowski (Stanford)

SEPTEMBER 9, 2022

Appendices

- TCAD (Victor Moroz, Fellow Synopsys)
- EDA (Prith Banerjee, CTO, Ansys)
- American Semiconductor Academy (Tsu-Jae King Liu, Dean UC Berkeley)
- NNCI Overview (Oliver Brand, Georgia Tech)
- Role of Universities (Jesus Del Alamo, MIT)
- Shaping the Future: Intel's Academic Collaborations (Gabriela Cruz Thompson and Sowmya Venkataramani, Intel)
- Workforce Development Overview (Peter Bermel, Purdue University)
- Workforce Development Panel (Patrick Govang, Cornell University)

White Paper: Microelectronics/Semiconductor Research Community Virtual Workshop

SUMMARY

In response to the recent efforts of the federal government to bolster US semiconductor manufacturing under the auspices of the CHIPS Act, the NSF's National Nanotechnology Coordinated Infrastructure (NNCI) held a two-day virtual workshop to examine how the NNCI can address various components of the CHIPS initiative.

The global semiconductor market is currently over $600B, with an annual growth rate of ~10%, and will drive a $3T electronics market by the end of decade. The US share of this market has fallen to less than 10%, which has clear economic and defense ramifications. This was the impetus for Congress to pass the $52B CHIPS legislation to encourage in-shoring of semiconductor fabs.

The first day of the workshop was devoted to invited talks by industry leaders who discussed the state of the art in their respective fields, and research challenges, highlighting opportunities for academic research. In the morning session, Dr. Kavalieros from Intel focused on advanced transistors for logic applications, Dr. Ramaswamy from Micron discussed advanced memory architectures, and Dr. Narayanan from IBM educated the attendees about heterogeneous integration (HI) as the next paradigm in Moore's law and Dennard scaling. Some of the common themes that emerged are the move toward next-generation 3D devices such as nanosheet transistors, and 2.5D and 3D HI of chiplets of CPU, GPU, high bandwidth DRAMs, and non-volatile memory using hybrid bonding with sub-10 micron pitch for applications such AI/ML using neuromorphic computing. Power management becomes a huge challenge in such 3D systems.

In the afternoon session, Dr. Chudzik from Applied Materials discussed equipment challenges for 300 mm tools which need to handle a wider set of materials, semiconductors beyond Si such as SiC and GaN, and advanced packaging. Dr. Moroz from Synopsys and Dr. Banerjee from Ansys discussed TCAD and EDA challenges, respectively. Moroz pointed out the need for more *ab-initio* simulation methodologies such as density functional theory (DFT) for structure calculations, coupled with non-equilibrium Green's function (NEGF) methodologies for electronic transport, which go beyond the usual drift-diffusion based simulators. Dr. Banerjee pointed out the need to do multi-physics simulations for HI, involving coupled heat and charge transport, as well as high speed simulation of Maxwell's equations to handle parasitics.

The industry overviews on the first day set the stage for sessions on the second day related to workforce development and academic infrastructure. For CHIPS legislation to be impactful, there must be significant renewal of aging academic microelectronics, R&D infrastructure, and a

1

National Nanotechnology Coordinated Infrastructure

Southwest

RTNN

ford

Microelectronics/Semiconductors Research Community

Report published December 2022

White Paper: Microelectronics/Semiconductor Research Community Virtual Workshop

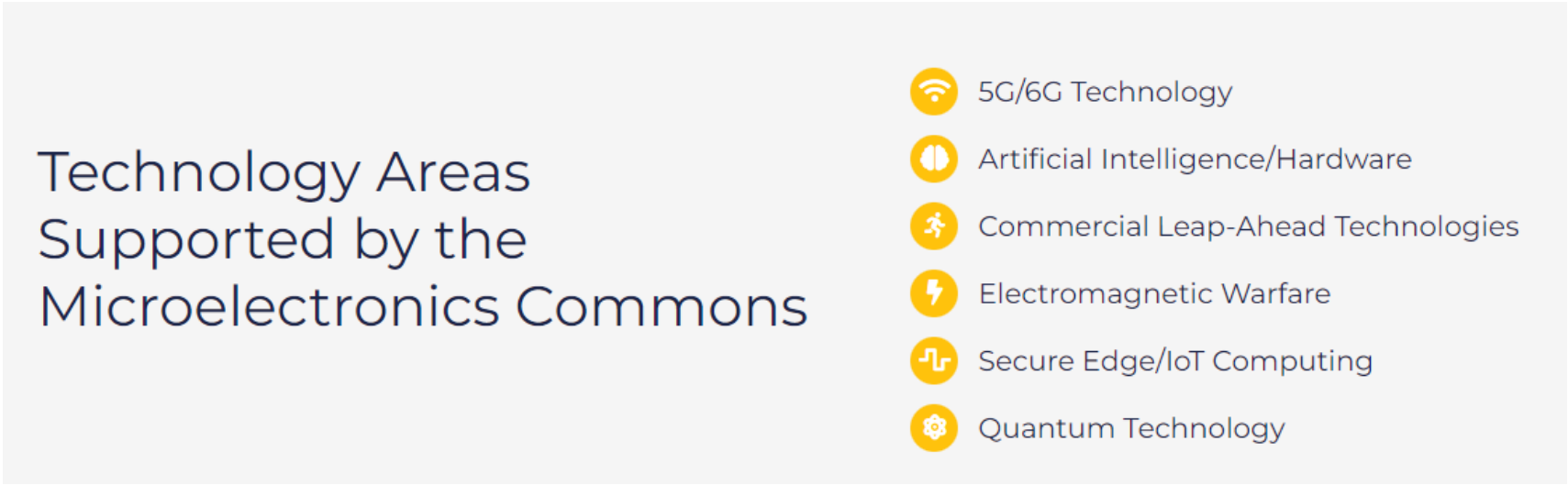
6: CONCLUSIONS / FUTURE DIRECTIONS

A key question that this workshop attempted to answer was how to revamp the aging academic cleanrooms. For example, what wafer size should universities target in the future, and how would these more expensive facilities be maintained? It may make sense to use CHIPS funding to build on the extremely successful NNCI model to expand the capabilities and geographical reach of NNCI. It was concluded that academic cleanrooms should not invest in 12-inch capability because of the expense of the equipment and operating costs. 8" may be the "sweet spot" where leading edge tools can be acquired and maintained at a sustainable cost. However, smaller wafer sizes such as 6" may also be a viable option for TRL 1 level work done by universities.

National Nanotechnology Coordinated Infrastructure NSF NCI Southwest TNF RTNN nano@stanford

Microelectronics/Semiconductors Research Community

Microelectronics Commons 'Request for Solutions' announced November 2022 with proposals due in February 2023



Eight regional Hubs announced in September

National Nanotechnology Coordinated Infrastructure

NSF

NCI Southwest

TNF

RTNN

nano@stanford

Microelectronics/Semiconductors Research Community

The Microelectronics Commons Hubs

The Microelectronics Commons program comprises eight regional Hubs, each focused on multiple technology areas and supported by their network of commercial innovators. If you are interested in learning more, register for the Microelectronics Commons Annual Meeting in Washington, D.C.

Applied Research Institute Silicon Crossroads Microelectronics Commons (SCMC) Hub	**AZ Board of Regents on behalf of Arizona State University** Southwest Advanced Prototyping (SWAP) Hub	**The Board of Trustees of the Leland Stanford Junior University** California-Pacific-Northwest AI Hardware Hub (Northwest-AI-Hub)	**Massachusetts Technology Collaborative** Northeast Microelectronics Coalition (NEMC) Hub
Midwest Microelectronics Consortium The Midwest Microelectronics Consortium (MMEC)	**North Carolina State University** Commercial Leap Ahead for Wide-bandgap Semiconductors (CLAWS)	**The Research Foundation for SUNY, acting on behalf of SUNY Polytechnic Institute** Northeast Regional Defense Technology Hub (NORDTECH)	**University of Southern California** California Defense Ready Electronics and Microdevices Superhub (California DREAMS)

https://microelectronicscommons.org/

Microelectronics/Semiconductors Research Community

The Microelectronics Commons Hubs

- The Northeast Microelectronics Coalition Hub. This hub is led by the Massachusetts Technology Collaborative in Massachusetts, has 90 hub members, and has been awarded $19.7 million.
- The Silicon Crossroads Microelectronics Commons Hub. This hub is led by the Applied Research Institute in Indiana, has 130 hub members, and has been awarded $32.9 million.
- The California Defense Ready Electronics and Microdevices Superhub Hub. This hub is led by the University of Southern California in California, has 16 hub members and has been awarded $26.9 million.
- The Commercial Leap Ahead for Wide Bandgap Semiconductors Hub. This hub is led by the North Carolina State University in North Carolina, has seven hub members and has been awarded $39.4 million.

National Nanotechnology Coordinated Infrastructure

https://www.defense.gov/News/News-Stories/Article/Article/3532338/dod-names-8-locations-to-serve-as-new-microelectronics-commons-hubs/

Microelectronics/Semiconductors Research Community

The Microelectronics Commons Hubs

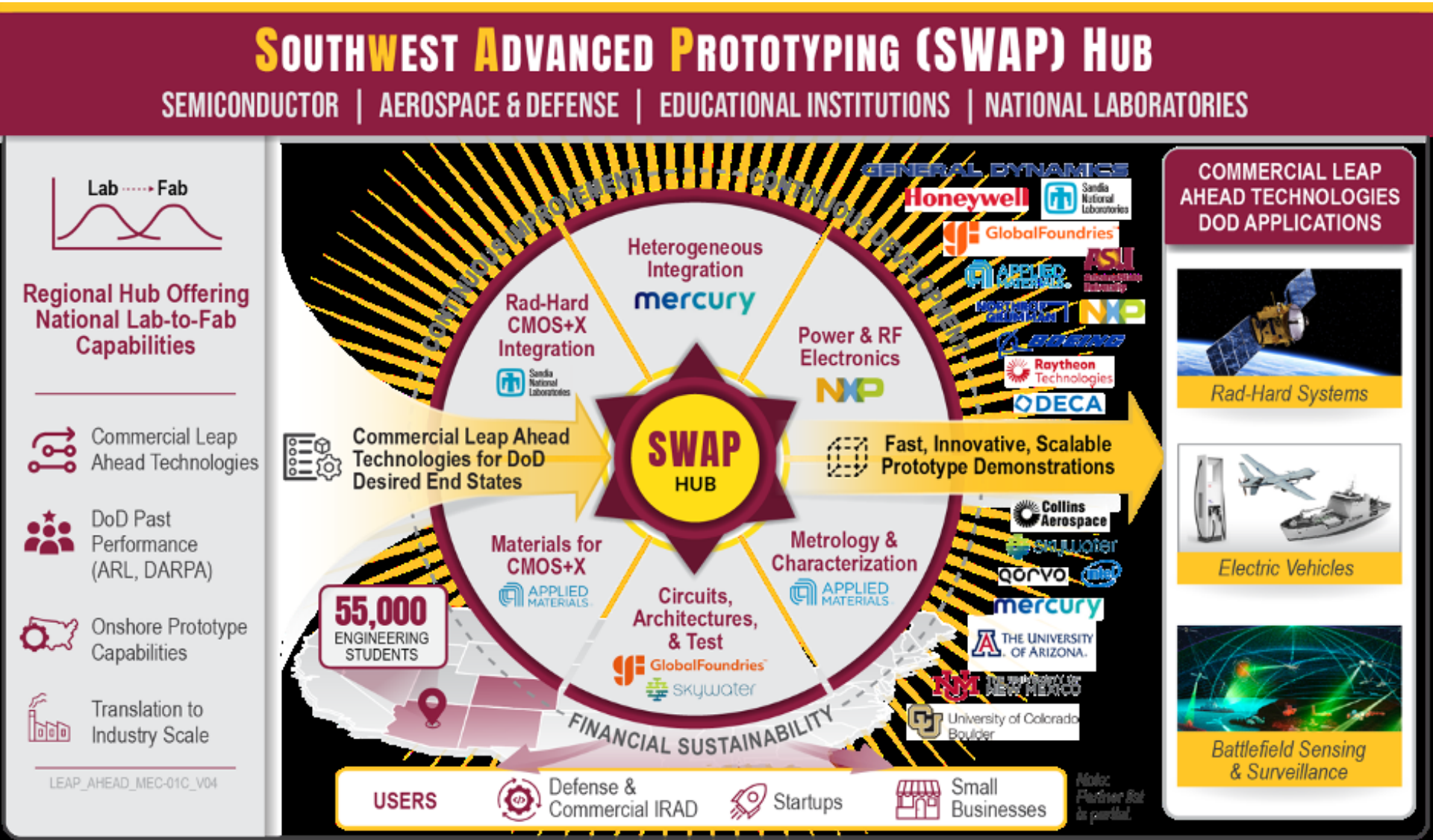
- The Southwest Advanced Prototyping Hub. This hub is led by the Arizona Board of Regents on behalf of Arizona State University in Arizona, has 27 hub members and has been awarded $39.8 million.
- The Midwest Microelectronics Consortium Hub in Ohio. This hub has 65 hub members and has been awarded $24.3 million.
- The Northeast Regional Defense Technology Hub. This hub is led by the Research Foundation for the State University of New York in New York, has 51 hub members, and has been awarded $40 million.
- The California-Pacific-Northwest AI Hardware Hub. This hub is led by the Board of Trustees of the Leland Stanford Junior University in California, has 44 hub members, and has been awarded $15.3 million.

National Nanotechnology Coordinated Infrastructure

https://www.defense.gov/News/News-Stories/Article/Article/3532338/dod-names-8-locations-to-serve-as-new-microelectronics-commons-hubs/

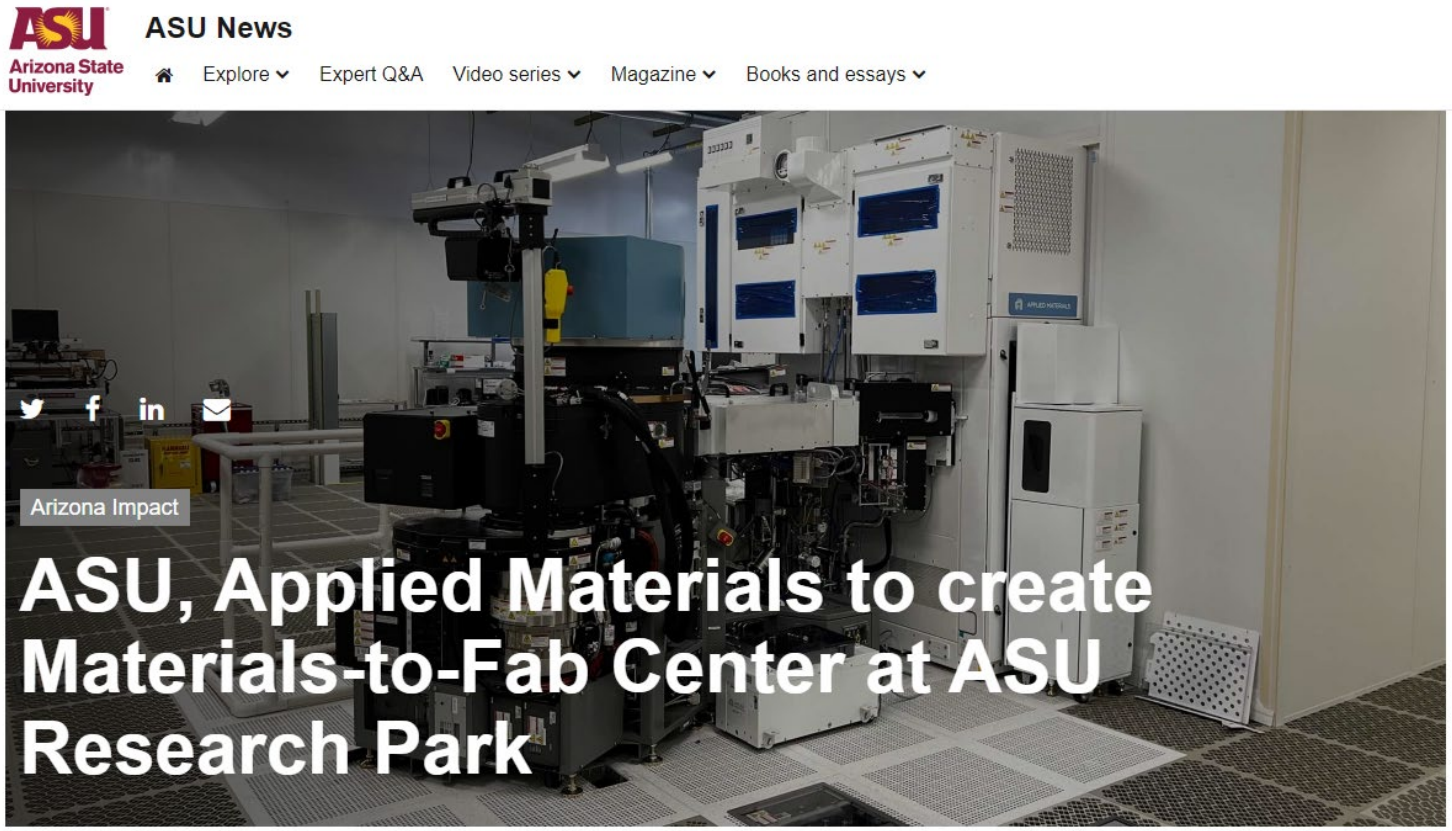
Microelectronics/Semiconductors Research Community

ASU SWAP Hub



Microelectronics/Semiconductors Research Community

ASU SWAP Hub



National Nc
Coordinate

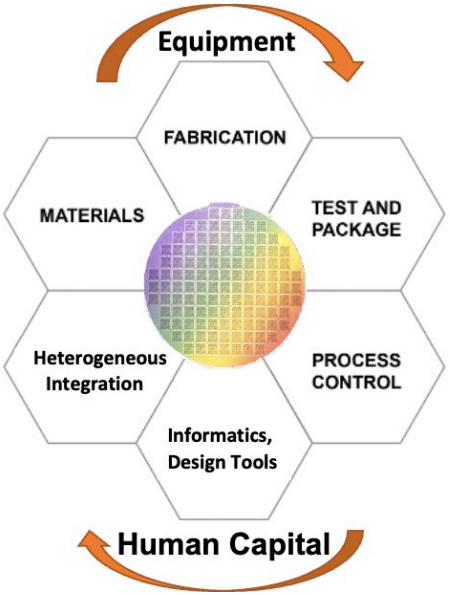
ıford

Microelectronics/Semiconductors Research Community

CLAWS Hub

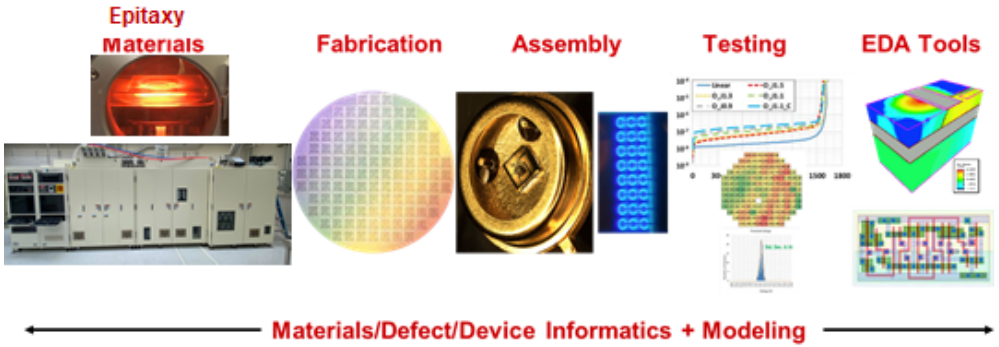
NC State, NC A&T State, Coherent, Wolfspeed, General Electric, Bluglass, Adroit Materials, Kyma

Wide Bandgap Semiconductor Research Foundry



Provide Low-Cost Agility in Semiconductor Development

Establish Critical Technology Roadmaps
Keep Constant Pulse on State of the Art
Identify and Leverage Synergies
Workforce with Technical Literacy



Silicon Carbide HV Electronics	III-Nitride UV-VIS Photonics
III- Nitride Electronics	Ultra Wide Bandgap Electronics

The desired end state is the lab-to-fab maturation of materials, devices, architectures, and processes to provide and/or enable revolutionary capabilities

National Nanotechnology Coordinated Infrastructure NSF NCI Southwest TNF RTNN nano@stanford

CLAWS Hub – Workforce Development

Proposed that Education and Workforce Efforts Scale with Prototype Projects to ensure relevance, involvement and sustainment of workforce activities.

Present Project Supports/Anticipates:

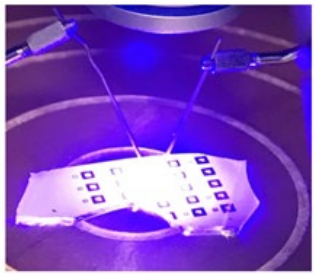
- Summer Programs at NCSU, NC A&T
- Specialized Short Courses
- Expanded Course involvement
- Community College Involvement
- Undergraduate Research
- Engagement with DOD SMART Fellowship Program.
- Outreach to K-12

- Intensive Training > 100 students/yea
- Exposure to Semiconductor Career opportunities > 1000 students/year.

Existing Workforce Development and Outreach Efforts

Research Foundry Creates Symbiotic Opportunity to Train Workforce

- Community College Trains the Trainer (Images this slide)
- Collaborate with Durham Tech., training Wolfspeed Technicians
- PowerAmerica Workshops, Equipment Short Courses
- 4 Undergrad and Graduate Courses with hands-on clean room
- Undergrad Work Study students assist in clean room operations
- Internships with Wolfspeed, other semiconductor companies
- Strong demand for NC State Students by Industry
- Undergrad research opportunities



Leveraging:

- NC A&T HBCU Expertise
- North Carolina Community College partnerships
- Regional Innovation Networks
- Industry Partners

Co-development of workforce

190+
Startups Launched

5K+
Invention Disclosures

600+
Products to Market

8.5K+
Total Jobs Created

1.5K+
Patents Issued

National Nanotechnology Coordinated Infrastructure

NSF

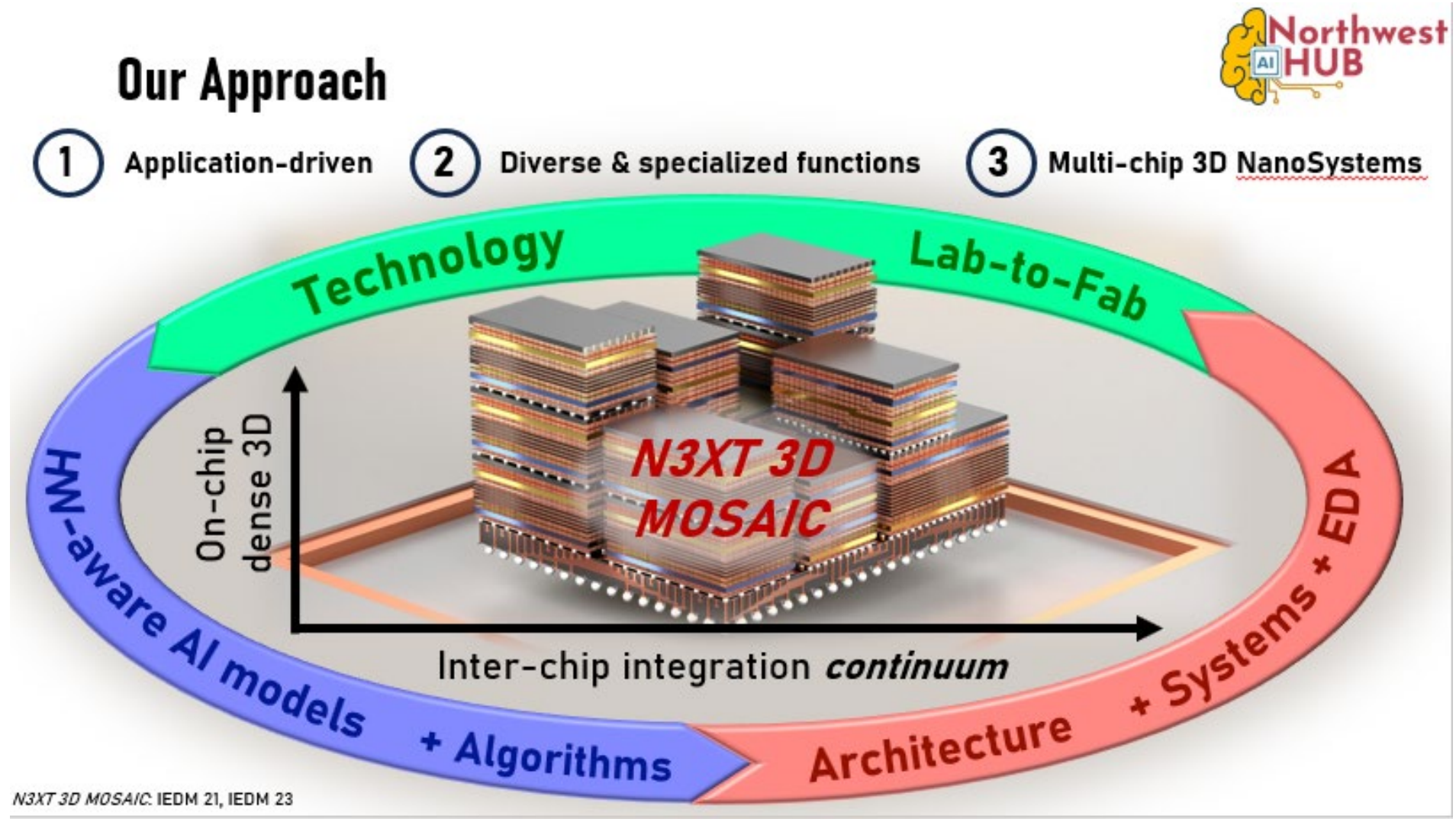
NCI Southwest

TNF

RTNN

nano@stanford

Microelectronics/Semiconductors Research Community



National Nanotechnology Coordinated Infrastructure

NSF

NCI Southwest

TNF

RTNN

nano@stanford

Microelectronics/Semiconductors Research Community

Northwest AI HUB

Hub Fab Facility Partners

Stanford University · Berkeley · Averatek · Western Digital · UC DAVIS · Lawrence Livermore National Laboratory

Commons Core Partners

SUNY Polytechnic Institute · MIT Lincoln Laboratory · intel · Global Foundries · IBM · AIM Photonics · skywater

Service Providers

Microsoft · Averatek · STNF · SIEMENS · CMTC · PLUGANDPLAY · imec · Lam Research · Ansys · SYNOPSYS · intel · Nhanced Semiconductors · Si Silicon Catalyst · MOSIS · Berkeley Lab · parc · Lawrence Livermore National Laboratory · cadence · SLAC National Accelerator Laboratory · NEXTFLEX

Workforce Development Partners

Stanford University · Berkeley · UC DAVIS · University of Washington · City College · SJSU San José State University · Sandia National Laboratories · Foothill College · CMTC · ARC American River College · Mission College Santa Clara · Si Silicon Catalyst · University of Hawai'i Maui · SAC State · NEXTFLEX · intel · Raytheon Technologies · SIEMENS · Lockheed Martin

Project/Research Partners

Stanford University · Berkeley · UC DAVIS · Oregon State University · University of Washington · Lam Research · Averatek · Lockheed Martin · University of Hawai'i Maui · parc · intel · Berkeley Lab · Lawrence Livermore National Laboratory · SLAC National Accelerator Laboratory · Raytheon Technologies · Western Digital · Global Foundries · SYNOPSYS · MIT Lincoln Laboratory · skywater · cadence · Collins Aerospace · NVIDIA · NEXTFLEX

Q&A