NCI Southwest

Central Arizona College

Integrated Tandem NanoFET Thermometers

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Background

- Field Effect Transistors (FETs) must become smaller in order to fit more of them into a given amount of space
- FETs now scaled down to sub-10nm dimensions and highly vulnerable to heat degradation
- Tackling device self-heating is key to improving the efficiency of silicon-based computing
- Applications include:
  - Direct sensory feedback within ICs
  - Improvement in wireless network speeds

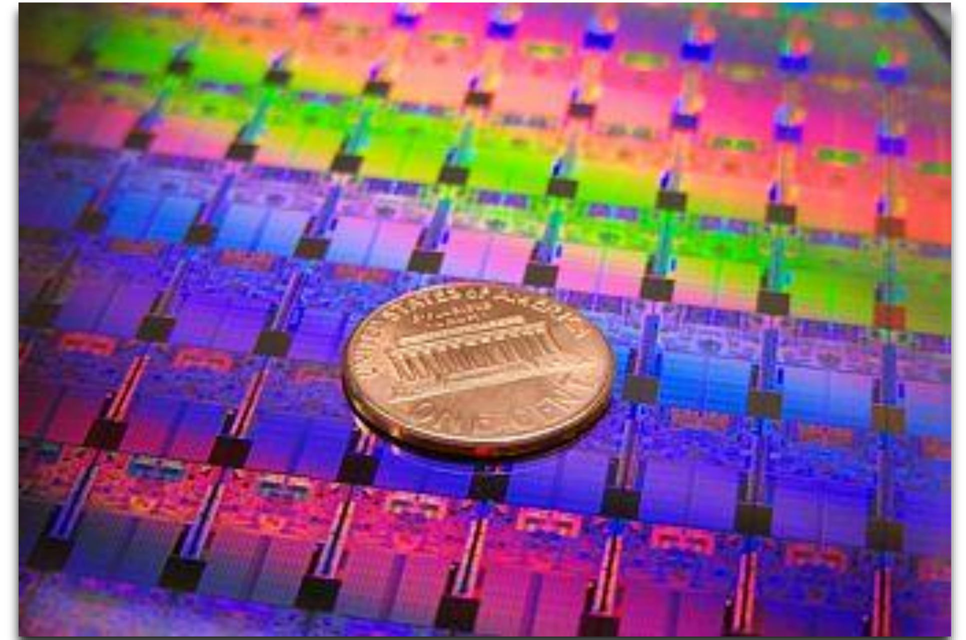
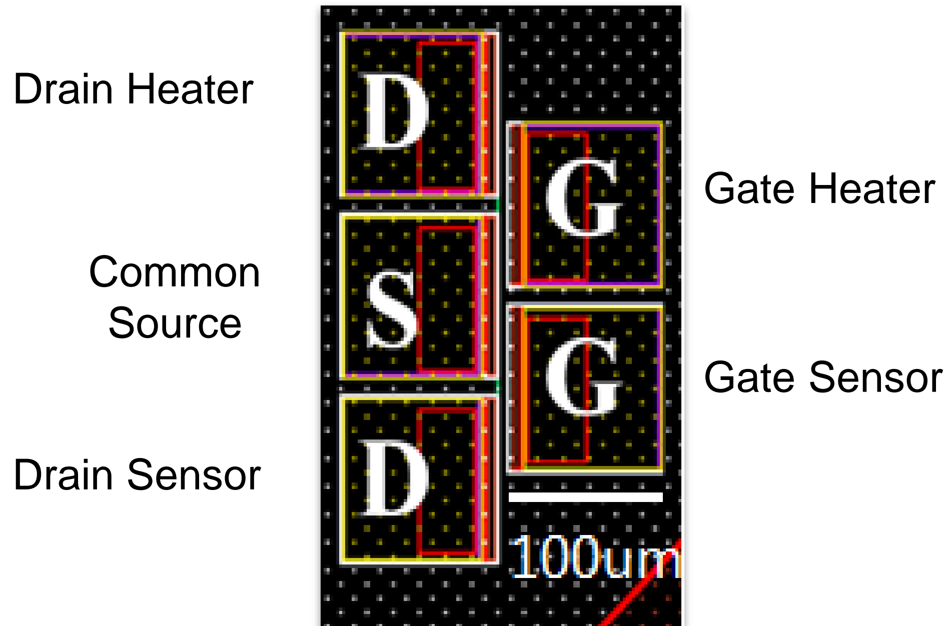


Figure showing a one cent piece on a sheet of single core processors. There are 410 million FETs on a single core. [1]

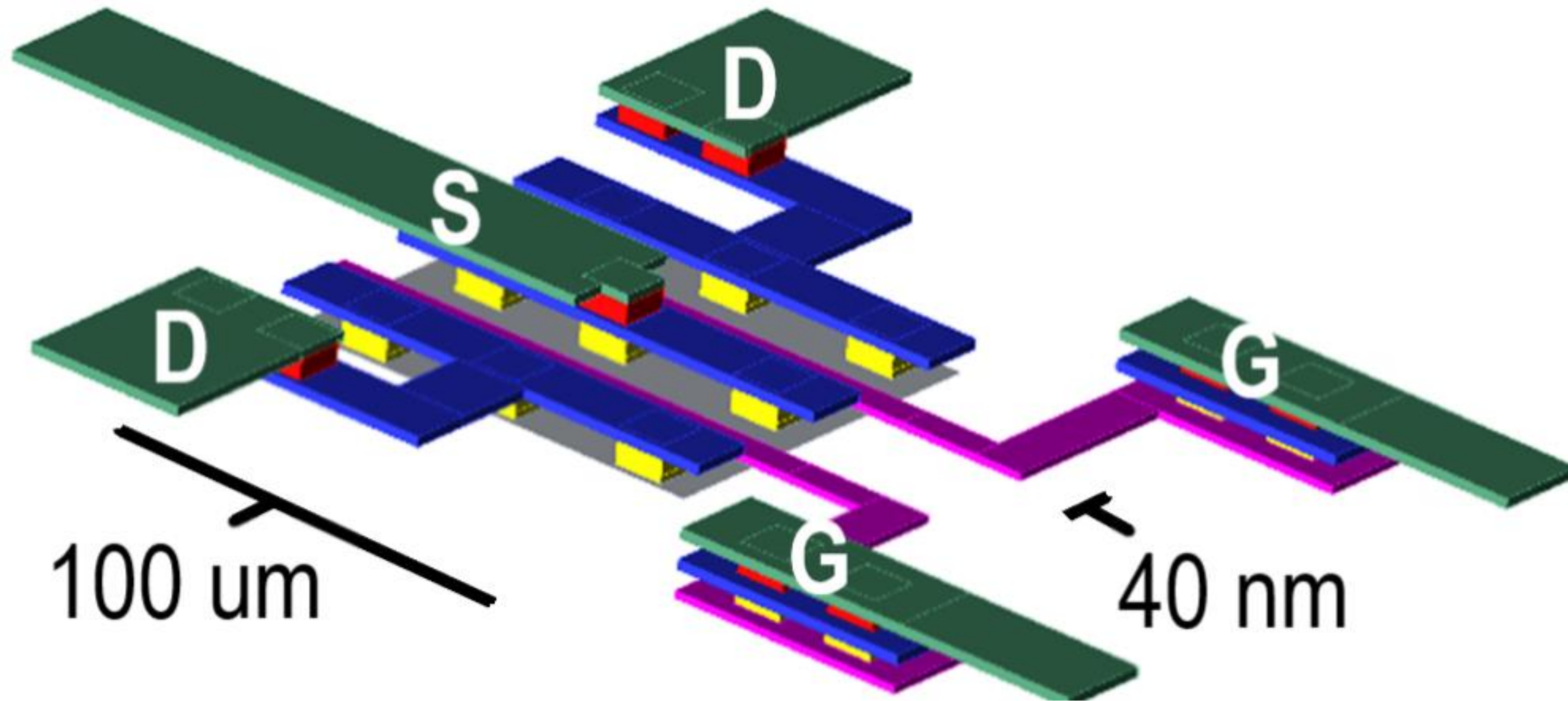
Introduction



D (Drain), S (Source), and G (Gate) are contact pads 100um in size compared to the 40nm FET

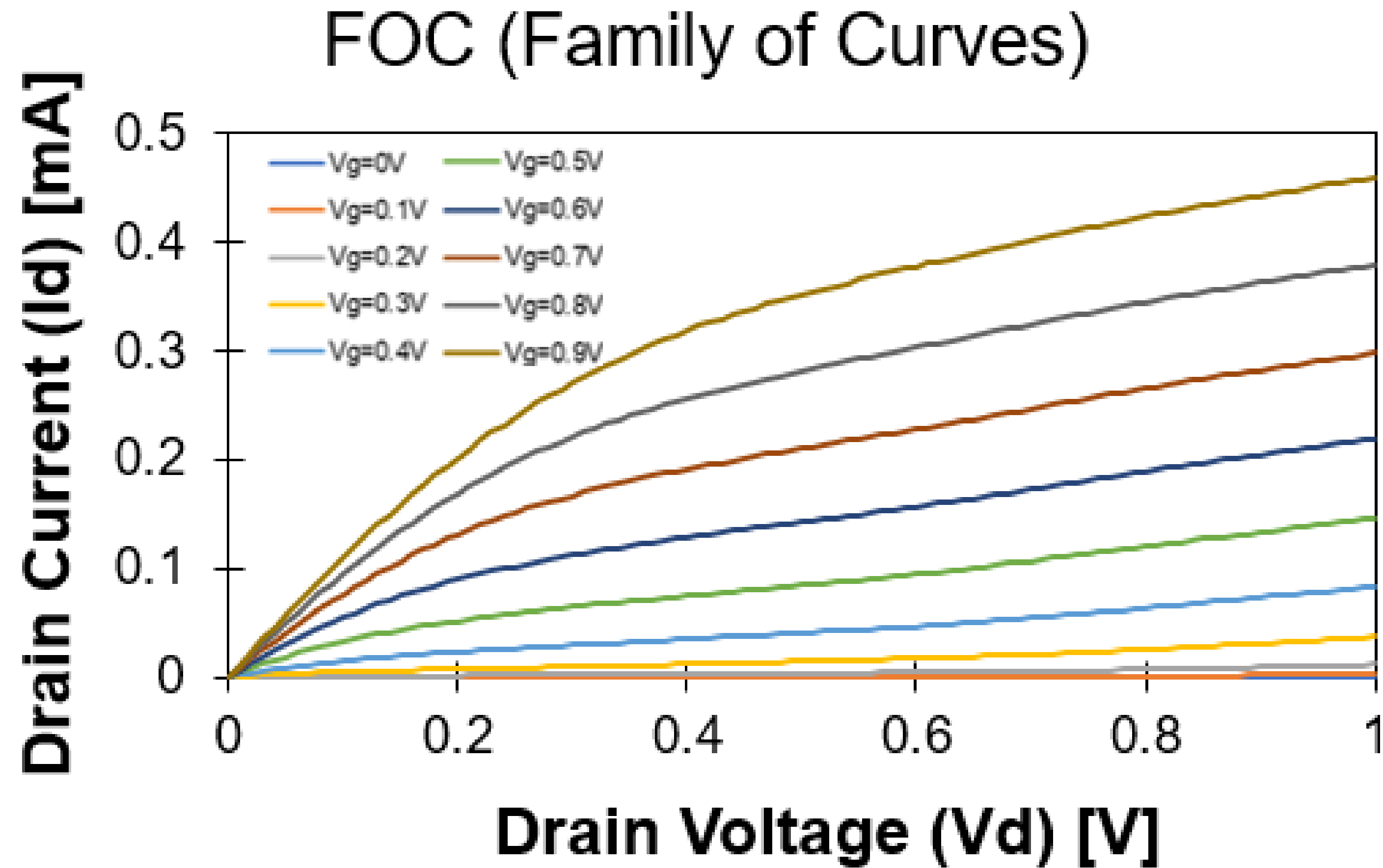
- Technique uses two adjacent FETs within the same IC as an integral thermometer
- When a small voltage is applied across the heater FET gate and drain contacts, the adjacent sensor FET increases in temperature and creates a measurable increase in the drain current of sensor FET
- Change in current can be used to calculate the increase in temperature of the heater FET
- Close proximity between the FETs = no heat lost during conduction, giving accurate results

Introduction



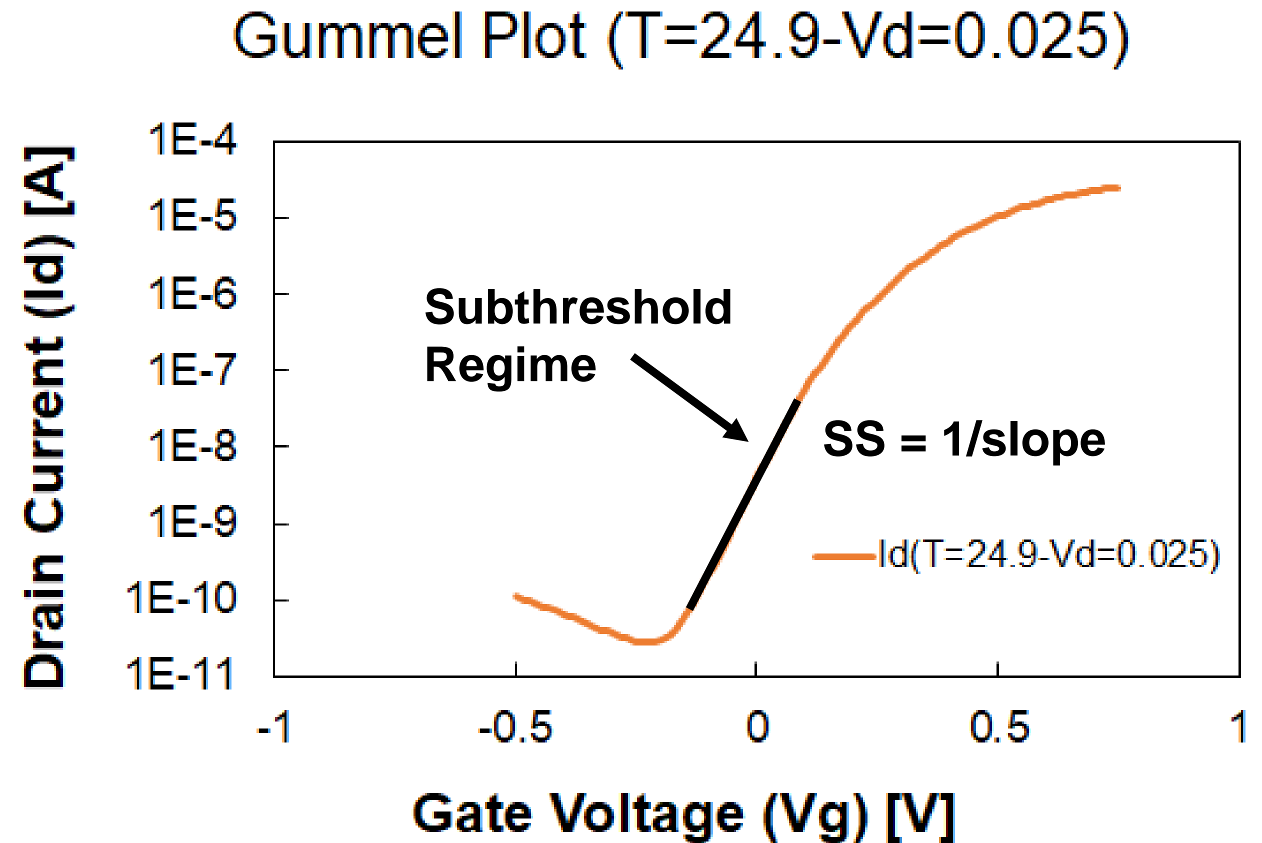
Methods; FET Response Curves

- FETs have a max drain current (Id) determined by drain voltage (Vd)
- Family of Curves (FOC) dictates which power settings to use during probe testing



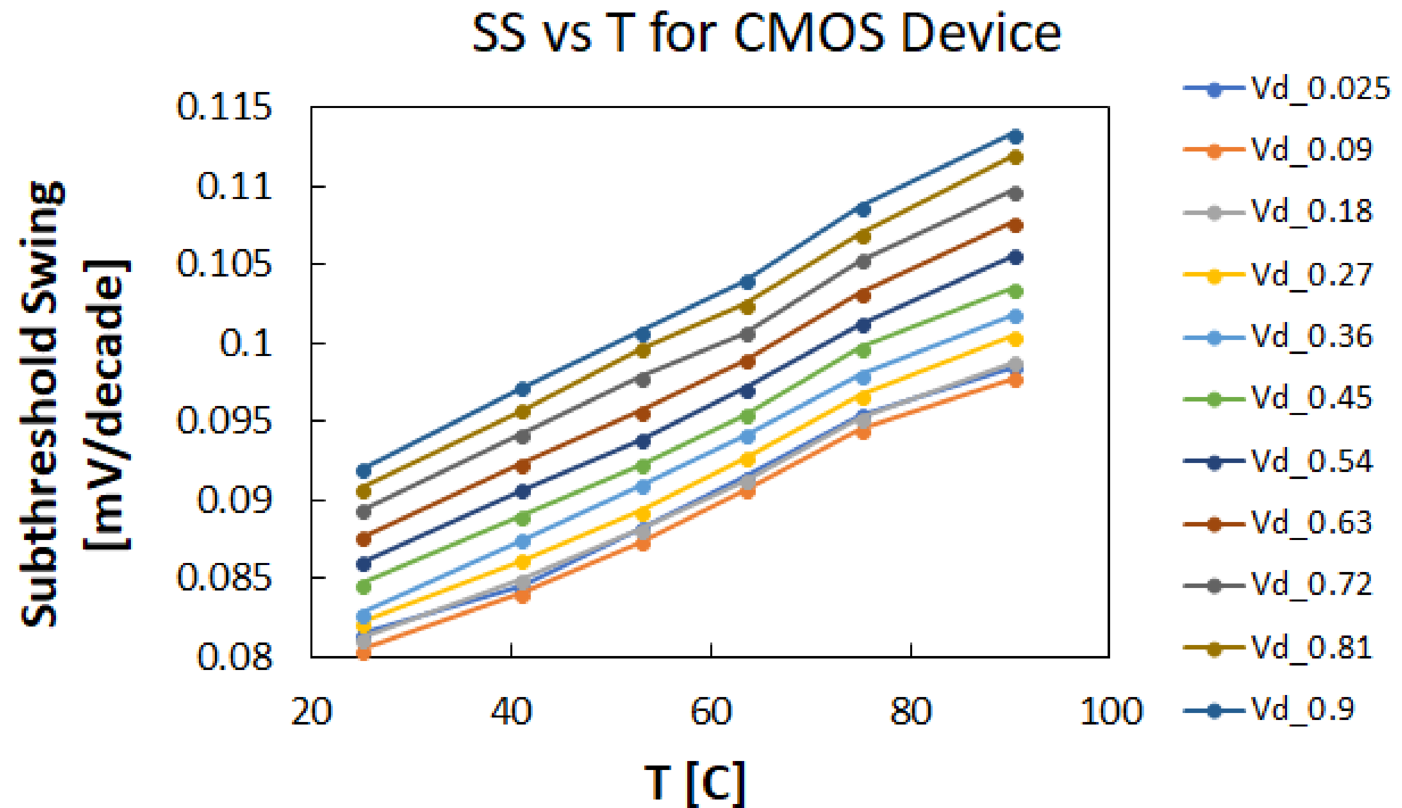
Methods; Gummel Plots

- Every FET has threshold gate voltage (Vth) determining turn-on characteristic
- Three-probe DC probing station sweeps gate voltage & measures drain current
- Beneath Vth is a “subthreshold regime,” drain current increases exponentially
- Subthreshold Swing (SS) = 1/slope of subthreshold plot



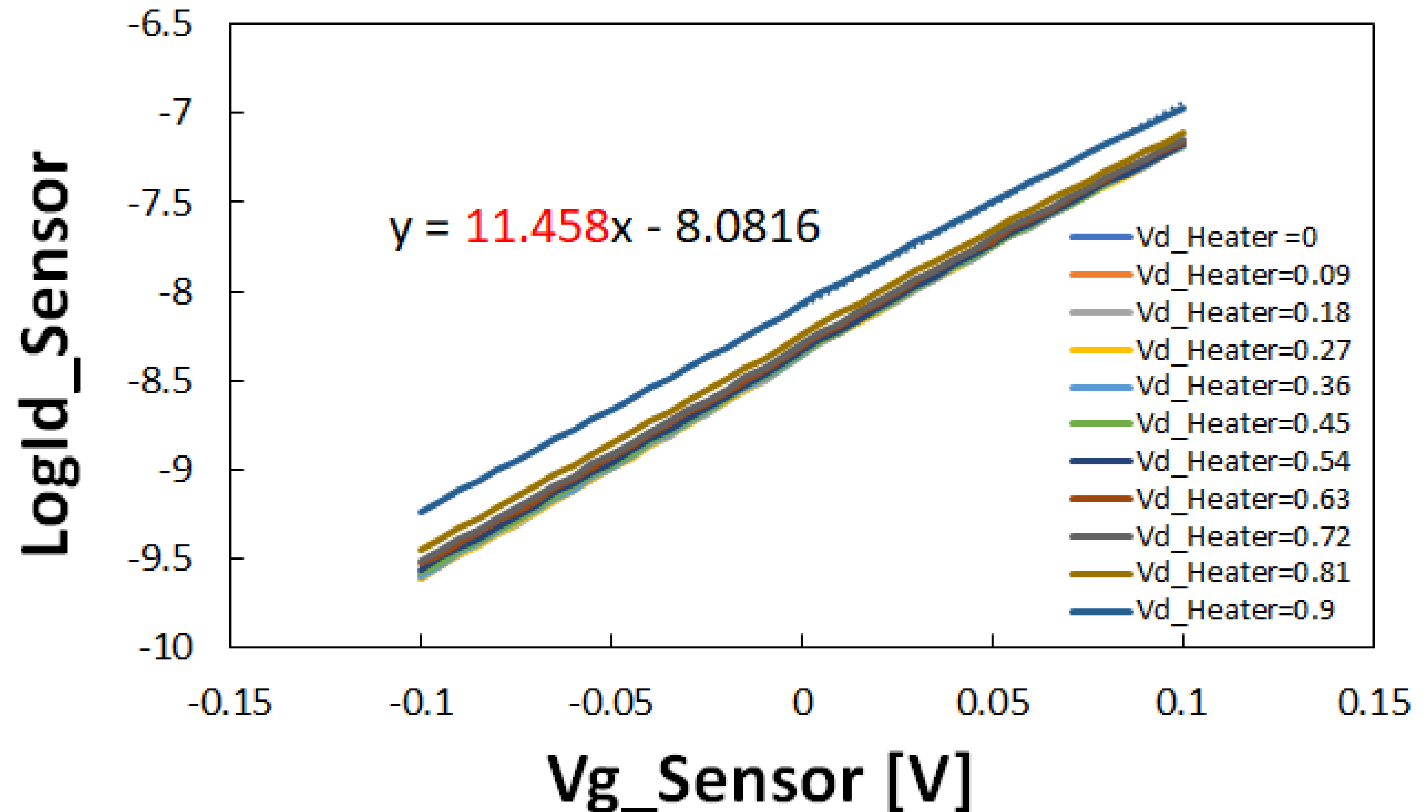
Methods; Thermometer Calibration

- Single FET tested on three-probe station
- Heated station chuck simulates heat from FET
- Multiple drain voltages serve to calibrate thermometer
- Plot shows SS vs chuck Temperature



Methods; Gummel Plot Slopes

- Five-probe DC probing station sweeps Vg_heater at increasing Vd_heater values and measures drain current of sensor FET
- Sensor FET's Gummel plot slopes extracted from graph of subthreshold regime on log scale & used to calculate T



Methods; Temperature Calculations

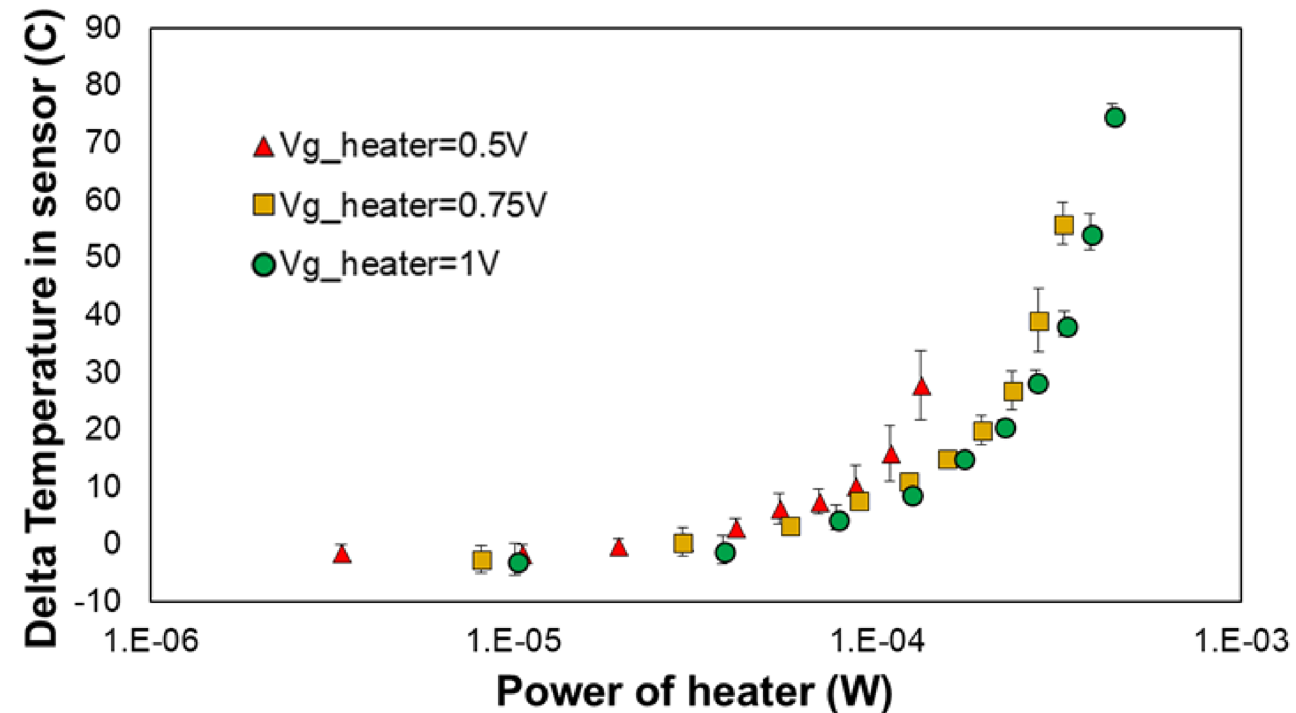
- Calculation for temperature
- Uses **slope** to find **Subthreshold Swing** (**SS** = 1/**slope**)
- **N** is a constant (~1.3)
- k = Boltzmann's Constant: 1.38×10^{-23} J/K
- q = Single electron charge: 1.602×10^{-19} C

T calc within subthreshold regime

$$T = \frac{(q)\left(\frac{SS}{N \times Ln(10)}\right)}{k}$$

Results

- Graph of multiple devices; power input vs average change in T with deviation in T between devices plotted as error bars
- Shows relationship between power generated and power lost as heat



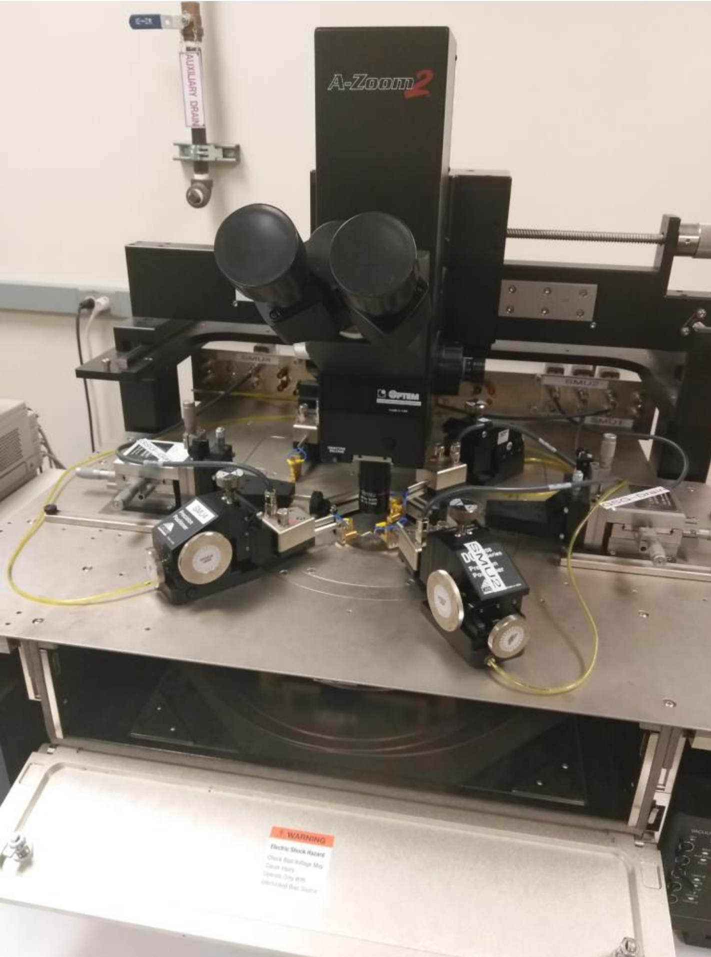
Conclusion

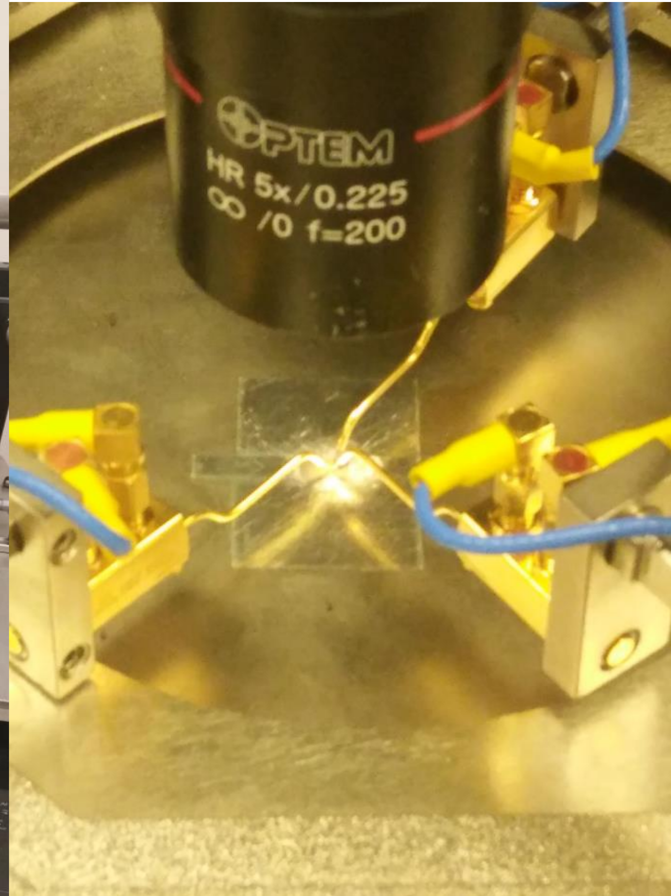
- IV measurements have confirmed our method for correlating heating to power generated in nanoscale FETs in a tandem, close-proximity configuration
- The data establishes a consistent method for correlating power consumption and heat loss within FETs
- Results are groundwork for digital models designed to predict the temperature change in many different types of FETs

References

[1] (Retrieved from: https://www.intel.com/pressroom/kits/45nm/photos.htm)
[2] E. Bury, et al. “Experimental validation of self-heating simulations and projections for transistors in deeply scaled nodes.” Published in: 2014 IEEE International projections Reliability Physics Symposium.

Questions?


A-Zoom2


OPTEM
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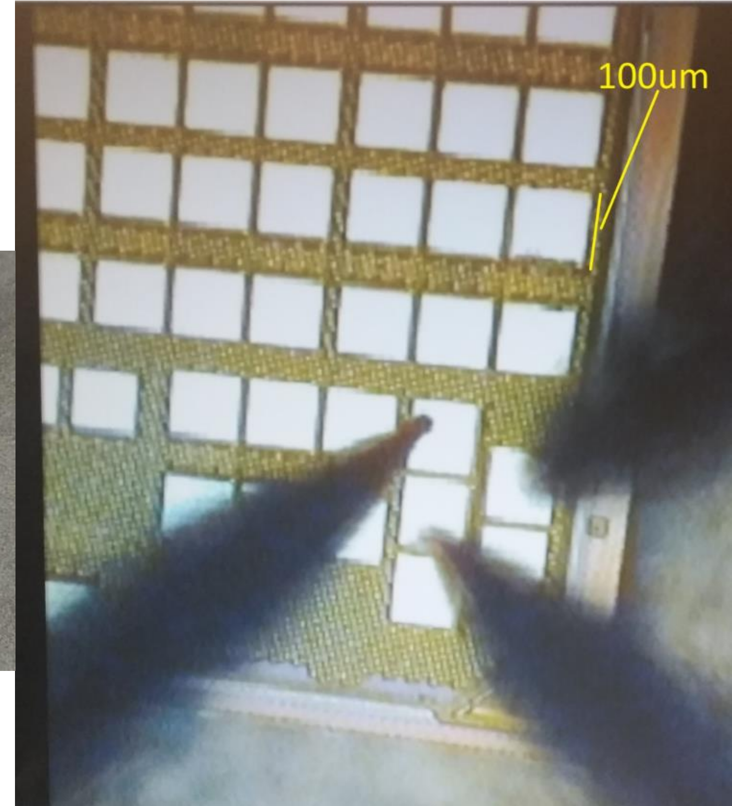
100um

$$I_D^{sat} = I_0 \exp\left(\frac{V_{gs}}{NkT/q}\right) \times exp(c)$$

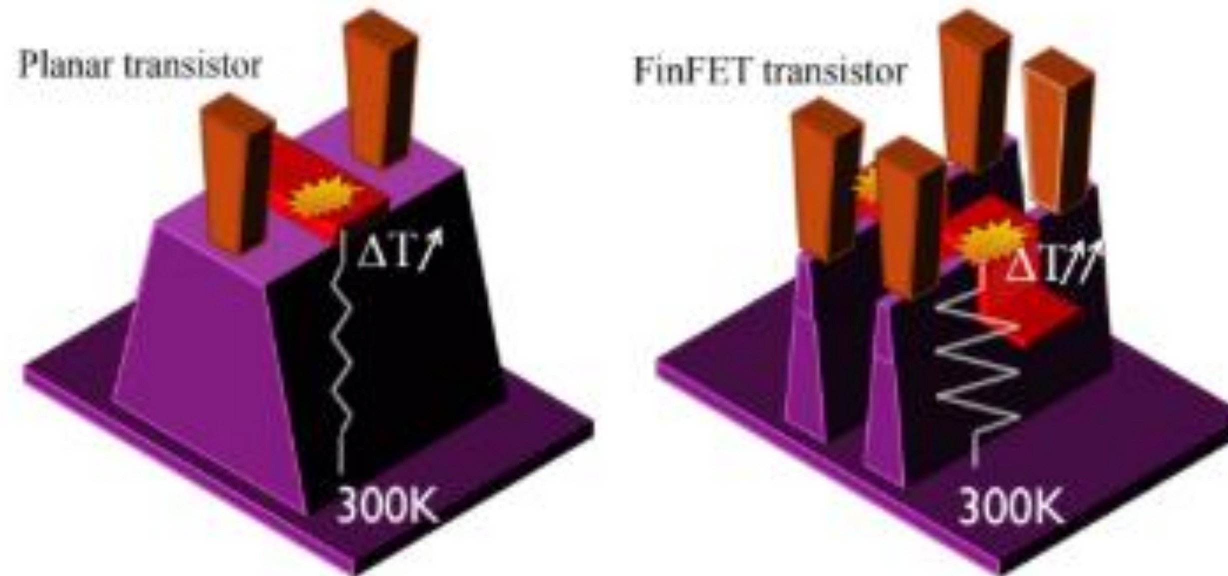

Figure showing that there is less silicon available for heat removal in modern FinFET devices, while the consumed power stays the same, or even increases [2].