Georgia Tech Institute for Electronics and Nanotechnology

Etching Equipment @ Georgia Tech

Team Leader: Vinh Nguyen

Process Engineer: Hang Chen
Equipment Engineer: Thomas Johnson-Averette

Nova Nanolab: Eric Woods
JEOL EBL: Devin Brown
Lasers : Richard Shafer

Cleanroom website:
http://sums.gatech.edu

Georgia Tech Institute for Electronics and Nanotechnology

STS Multiplex ASE DRIE (2001)

Pettit Cleanroom

Functions

- Deep Silicon Trench Etching (Bosch)
- SOI Wafer Etching

Substrates and Masks

- Substrates: Si, poly-Si, a-Si
- Mask: Resist, SiO_2, Si_3N_4
- No SU-8

Specifications

- Coil: 1000W 13.56 MHz ENI ACG-10B
- Platen:
  - HF: 500W 13.56 MHz ENI
  - LF: 300W 380 kHz AEI
- 8-pin ceramic clamp for 100mm w/ HBC Lip Seal
- Gases: C_4F_8, SF_6, O_2, Ar
- Process Pressure: 2 – 80 mTorr
- Temperature: 5-40 C (platen), 40 C (walls), 45 C (lid)

Vendor Specifications

- 30:1 aspect ratio 1um trench
- 15:1 aspect ratio 1um SOI w/ minimal notching

Actual Installation Results

- 43:1 aspect ratio 1um trench gratings

Recent Service/Modifications

- Kalrez seals for throttle valve
- Chamber liner laser cleaning through Pen-Tec

Georgia Tech Institute for Electronics and Nanotechnology

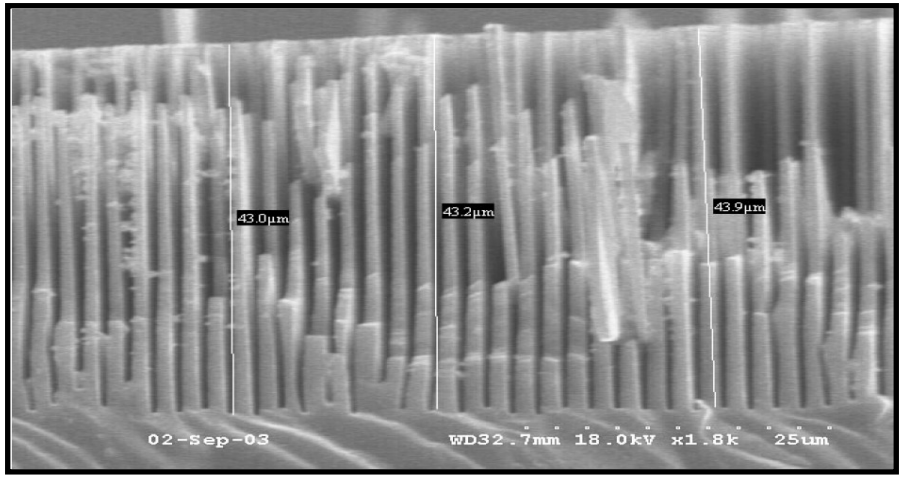
STS DRIE ASE Results:

Image provided by Eric Woods, P.I. James Zhou, Erin Walters IEN

- SiO_2 mask
- High gas flow rates
- Higher etch to passivation step times ratios
- Lower platen power

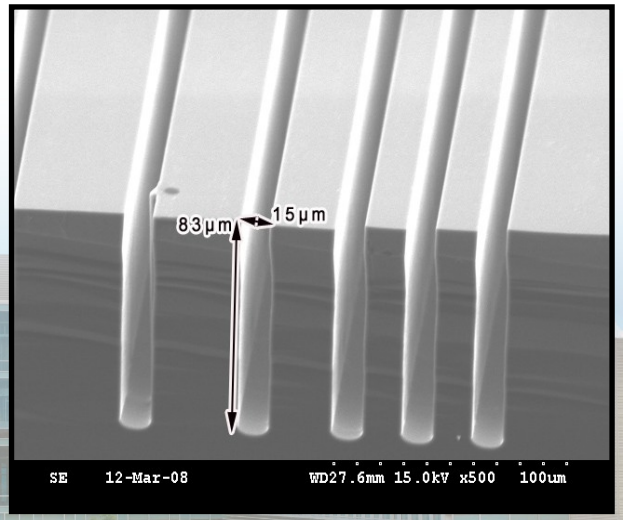
*Damage shown to trench sidewalls caused by cleaving process. Fins were prone to breakage, so trenches were partially filled with SiO_2, cleaved, then released using HF and a supercritical CO_2 drying process.

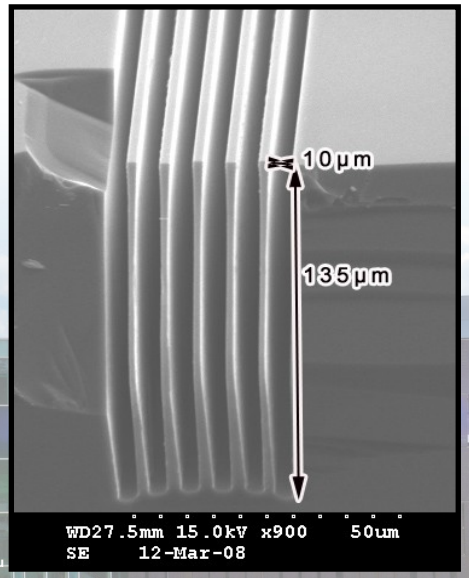
Best Results* - 43:1



Rules:

- Silicon etching only
- No exposed metal
- CMOS compatible only
- No through-wafer w/o carrier
- Backside of wafer must be clean





STS MULTIPLEX DRIE AOE (2006)

Pettit Cleanroom

Functions:

- High aspect ratio etching with high etch rate and selectivity

Materials etched and acceptable masks:

- Etched: SiO_2, quartz, Pyrex, fused silica, Si_3N_4, bulk silicon
- Masks: Si, PR & Metals (Cr, Ti, Ni)

Component specifications:

- 3000W 13.56MHz AE – Coil
- 1000W 13.56MHz ENI – Platen
- Backside Helium Cooling with Standard 8-pin clamp & lip seal

Gases: C_4F_8, SF_6, O_2, H_2, CF_4, two open gas slots

Process Pressure: 2-80mT

Substrate size: small pieces - one 150mm wafer

Temperatures: Platen -20°C to 120°C, Walls 100°C, Lid 120°C

Vendor Specified Capabilities:

- 2.5µm isolated trenches on 8-10µm TEOS
- Etch rate >2000Å/min SiO_2, >4:1 selectivity SiO_2: PR, etch rate variability intra- and inter-wafer ±3%, sidewalls 85-90°

Actual capabilities when tool acquired

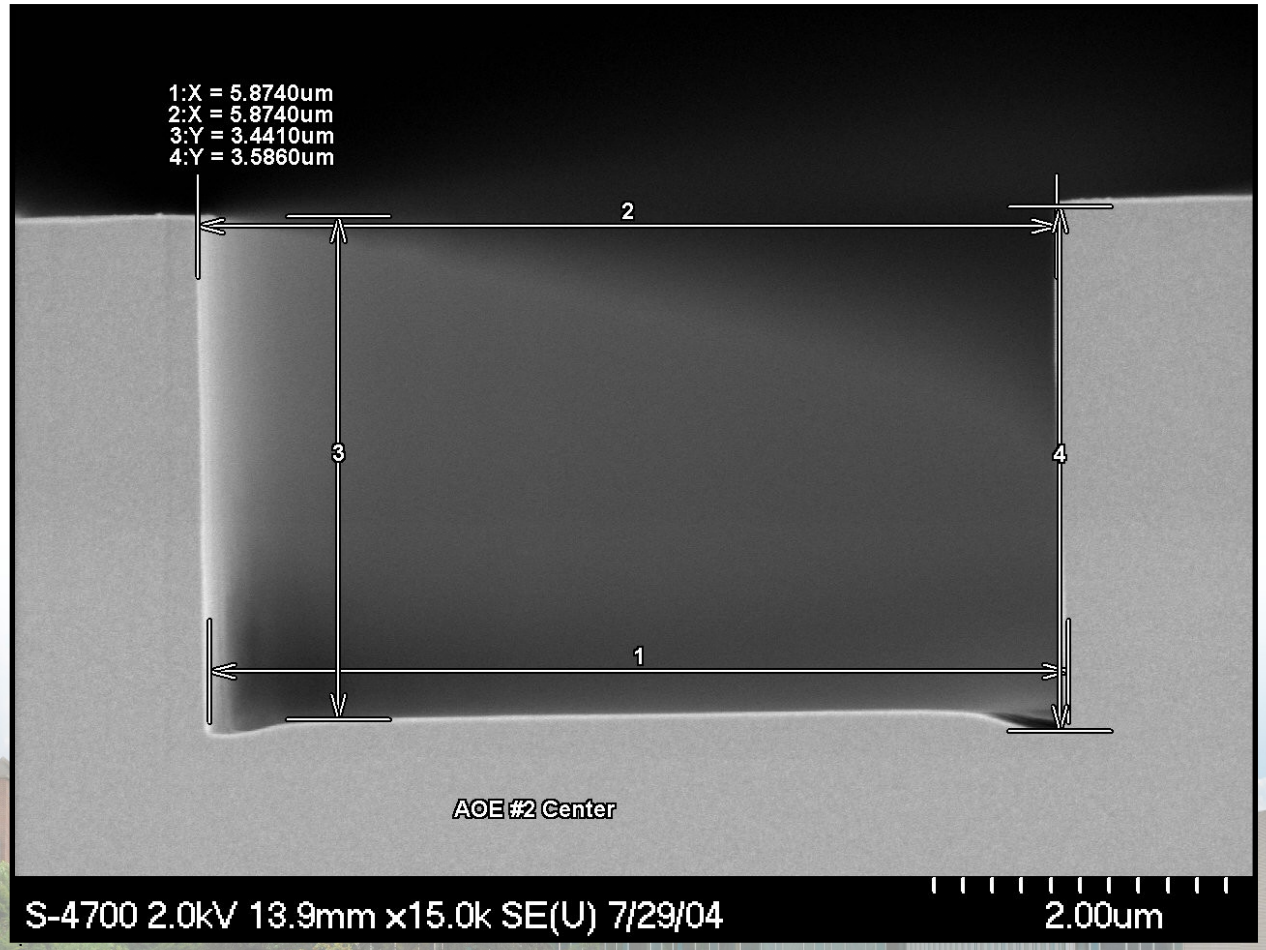
- 5µm features on 3-10µm SiO_2
- Etch rate >3000Å/min SiO_2, >7.5:1 selectivity SiO_2:PR, etch rate variability intra- and inter-wafer ±2%, sidewalls 89-90°

Recent Service/Modifications

- Converted to 100mm w/ ceramic parts (from quartz)
- Custom rebuild of matching network because of archaic gas cap failure

STS DRIE AOE examples

Images provided by Greg Kally, Mary Winters, and Judy Sline, Infotonics and Jeff Hawks, STS



Images from AOE process qualification August 2, 2004

Gases: C_4F_8, H_2

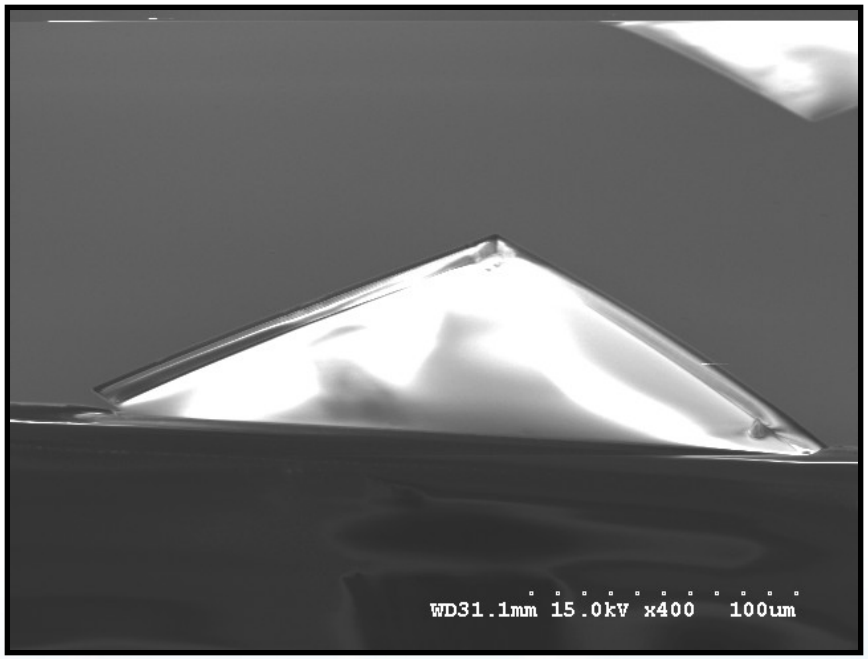
Pressure: 4mTorr

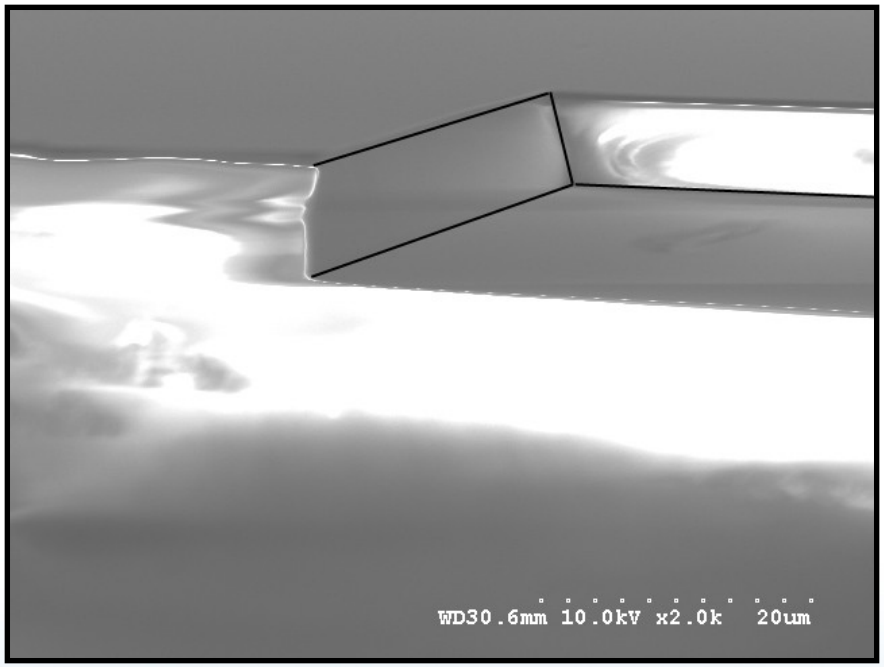
Temp: -10°C

Small microtrench formation at bottom of trench

STS DRIE AOE: chrome mask

Images provided by Xin Gao. PI: Farrokh Ayazi, GT ECE





Chrome etch rate	323Å/min
Pyrex etch rate	0.282µm/min
Selectivity	25.6 : 1

Sample: Etched Pyrex with Cr removed

Feature size: 150µm

STS DRIE SOE (2006)

Pettit Cleanroom

Functions

- Shallow Silocon trench etching
- III-V etching

Substrates and Masks

- Substrates: SiO_2, Si (<10um)
- Mask: Resist, SiO_2, Si_3N_4, III-V

Specifications

- Coil: 1000W 13.56 MHz ENI
- Platen: 300W 13.56 MHz ENI
- 8-pin ceramic clamp for 100mm w/ HBC Lip Seal
- Gases: CH_4, H_2, Cl_2 BCl_3, HBr, CHF_3, CF_4, Ar, O_2, N_2
- Process Pressure: 2 – 80 mTorr
- Temperature: -20 - 180 C (platen), 40 C (walls), 45 C (lid)

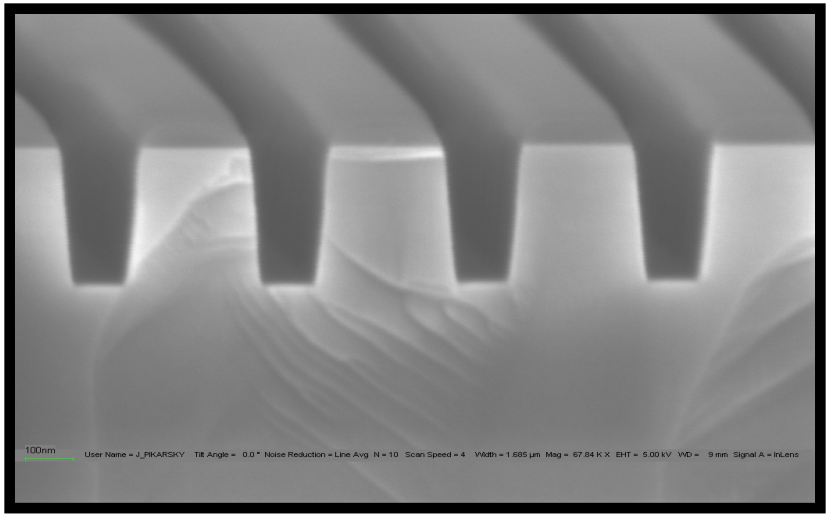
Recent Service/Modifications

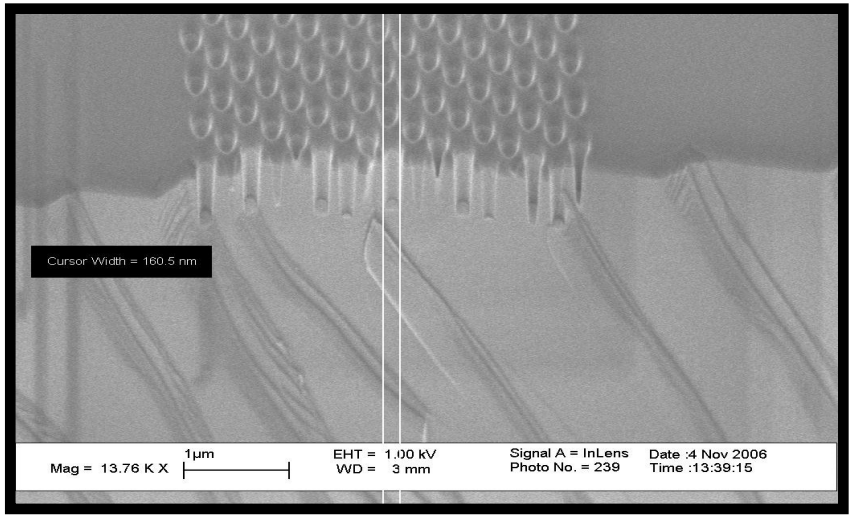
- Clamps added to improve loadlock pumpdown
- Several boards/terminals replaced troubleshooting LL issue

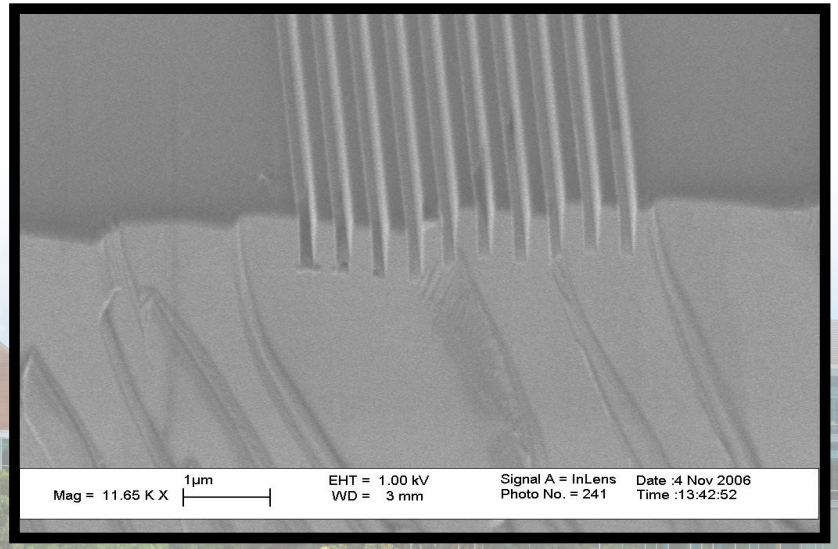
Georgia Tech Institute for Electronics and Nanotechnology

STS DRIE SOE: GaN

Images provided by Ehsan Hosseini. PI: Ali Adibi





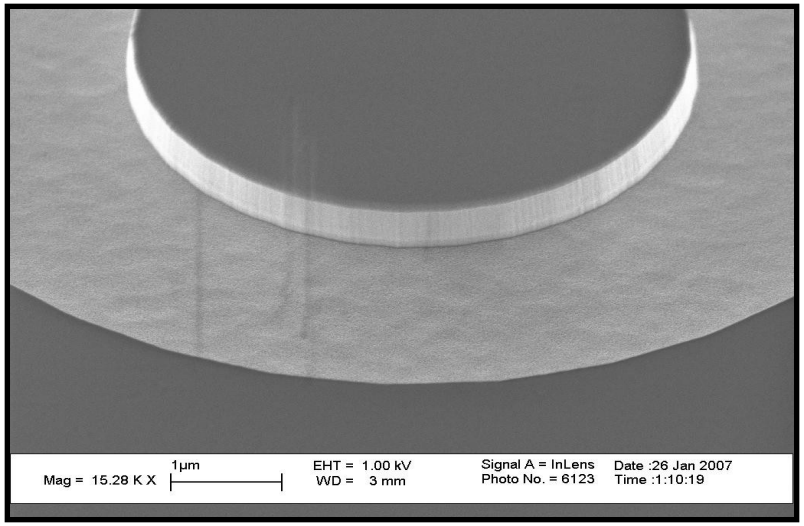


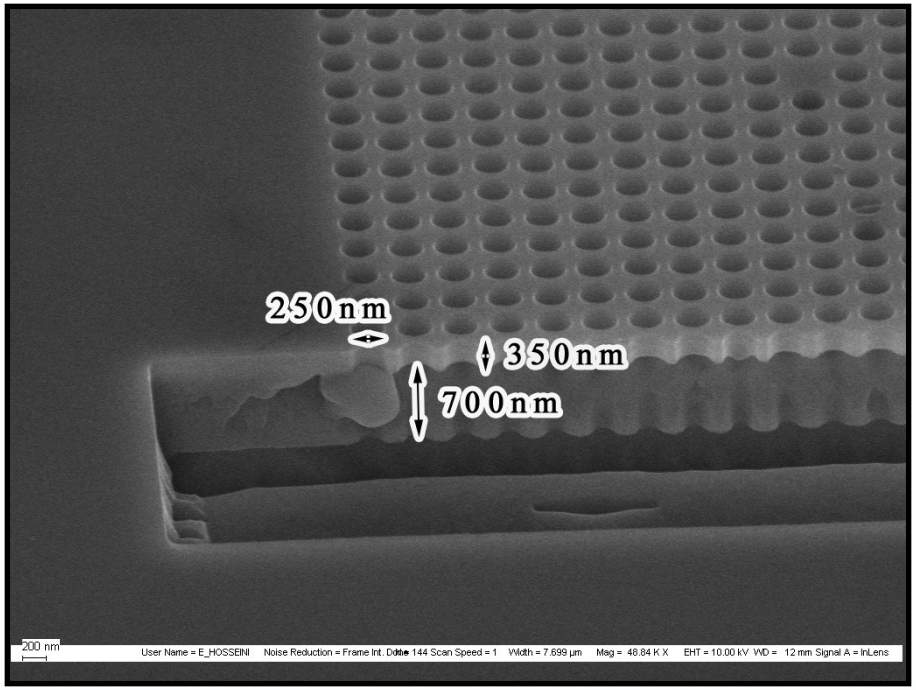
- Gases: Cl_2
- Mask: SiO_2
- Grating Structure

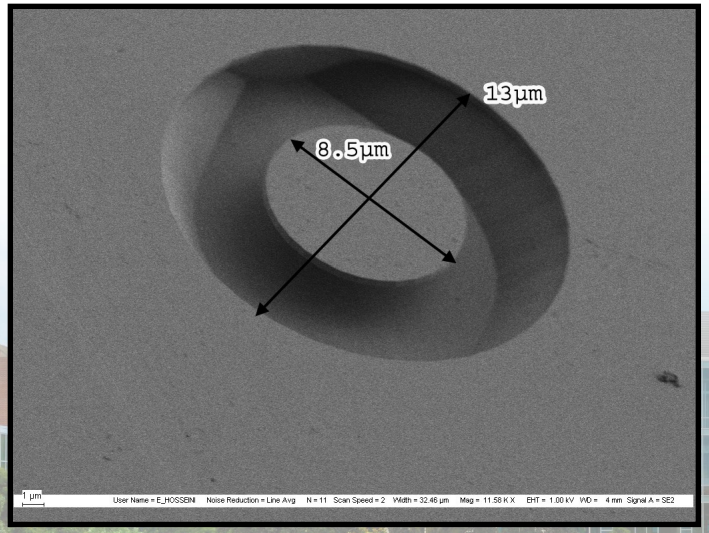
Georgia Tech Institute for Electronics and Nanotechnology

STS DRIE SOE: InAlGaAs

Images provided by Ehsan Hosseini. PI: Ali Adibi







- Gases: BCl_3, CH_4, Ar
- Mask: SiO_2 / Si_3N_4
- Photonic Crystal

STS ICP ASE Pegasus (2008)

Pettit Cleanroom
Tool Currently Installed / STS Qualifying Processes

Function:
- Silicon Trench Etching (Bosch process)
- First Pegasus installed in US university

Materials etched and acceptable masks:
- Etched: Si, poly-Si, α-Si
- Masks: Photoresist, Si_3N_4, SiO_2

Component Specifications:
- 5000W 13.56MHz MKS – Coil
- 500W 13.56MHz ENI -- Platen
- 300W 380kHz AE LF-5
- Backside helium cooling with electrostatic chuck

Gases: C_4F_8, SF_6, O_2, Ar

Substrate size: small pieces – one 100mm wafer or 150mm capability

Process Pressure: 2-80mT

Temperatures:
- Platen -20°C to 40°C, Walls 120°C, Lid 120°C

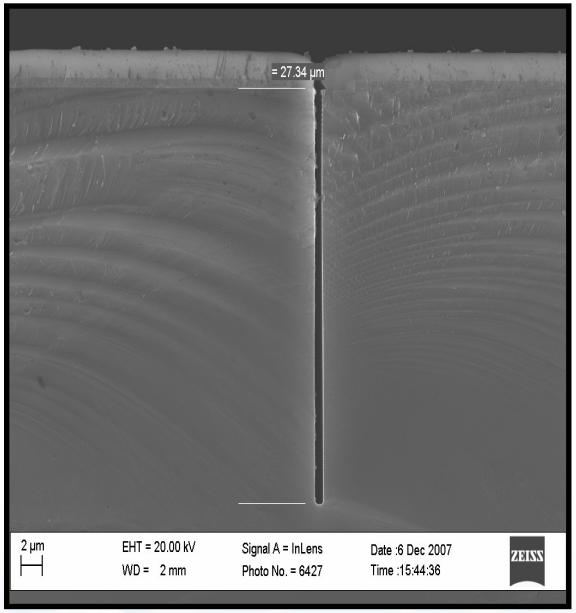
Vendor Specified Capabilities with 10% exposed Si (Width : Trench Depth):
- 0.5µm : 30µm SOI (LF platen)
- 0.2µm : 10µm SOI (LF platen)
- 3µm : 100µm (HF platen)
- 2µm : 60µm (HF platen)

Tool Scheduled to be moved to Marcus Cleanroom

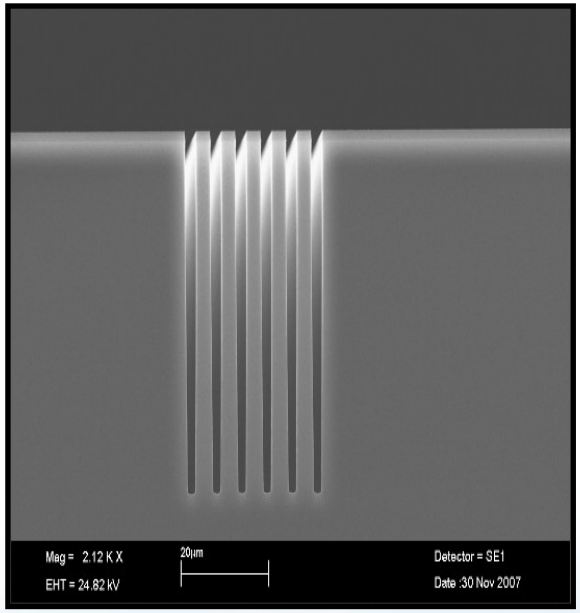
Georgia Tech Institute for Electronics and Nanotechnology

STS DRIE ASE Pegasus Examples

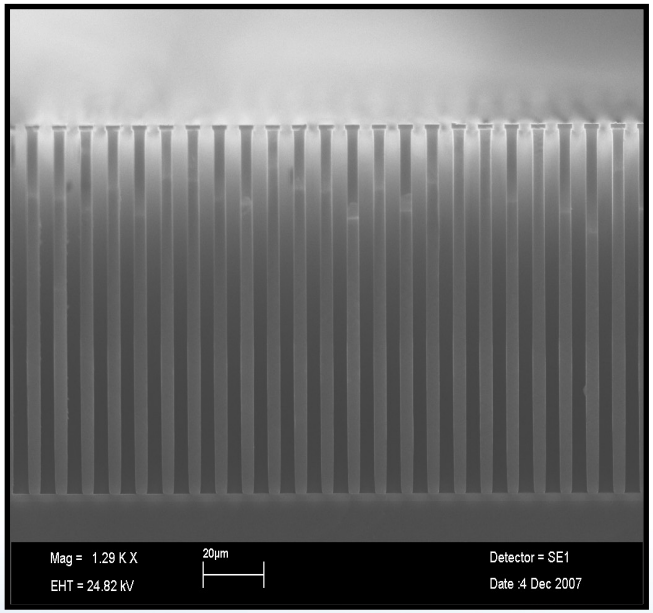
Images provided by Varun Keesara & Prof. Farrokh Ayazi



Width:Trench Depth
0.5µm:27µm



Width:Trench Depth
2µm:60µm



Width:Trench Depth
3µm:100µm

PlasmaTherm Dual DRIE SLR (1995)

Pettit Cleanroom

Dual Chamber Etching System Featuring:

- (Right) Si trench etch / poly-Si / through-wafer
- (Left) III-V etching; SiO_2 Si_3N_4 & Al / metal etching

Materials etched and acceptable masks:

- Etched/Left: SiO_2, Si_3N_4, Al, III-V → InP, InGaAs
- Mask/Left: Metal, Photoresist
- Etched/Right: Silicon, poly-Si
- Mask/Right: no metal masks (only PR, Si_3N_4, SiO_2)

Component specifications (both):

- Coil: 2000W 2.8MHz RFPP RF-20M
- Platen: 500W 13.56MHz RFPP RF-5S
- HBC: Both chambers
- Left: Ceramic Clamp; Right: ESC

Gases:

- Left: Cl_2, BCl_3, C_4F_8, CF_4, H_2, Ar, O_2
- Right: SF_6, O_2, C_4F_8, Ar

Process Pressure: (5-80mTorr both chambers)

Substrate: small pieces - one 100mm wafer, up to 150mm in right chamber

Temperatures:

- Platen: Left 20°C; Right 20°C
- Chamber: 40°C

Recent Service/Modification:

- Right chamber HBC leak repaired
- Full platen PM for both chambers (seals, lift, cleaning)

PlasmaTherm DRIE-Bosch results

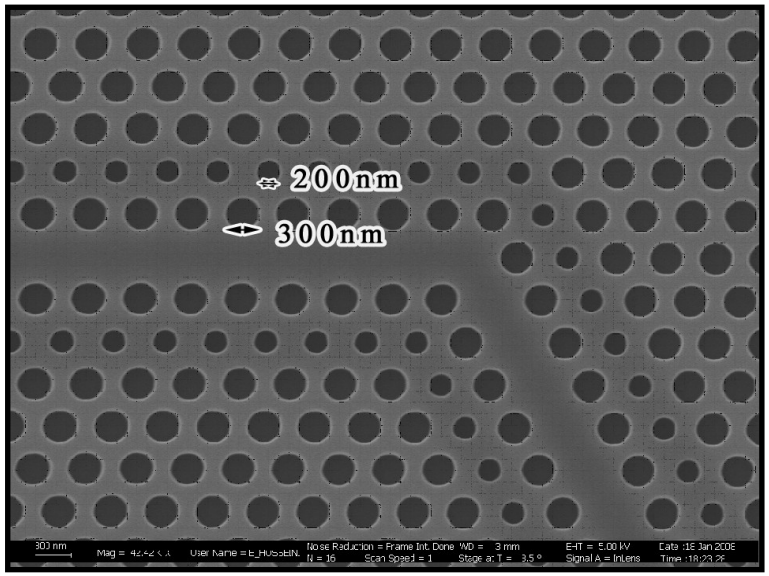
Images provided by Florian Herrault. PI: Mark Allen (left) and Ehsan Hosseini. PI: Ali Adibi (right)

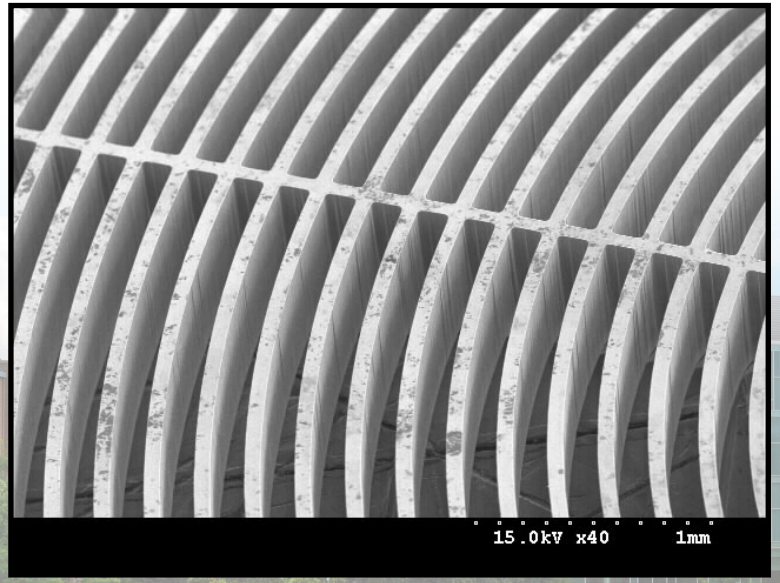
Si Trench Etch – left image:

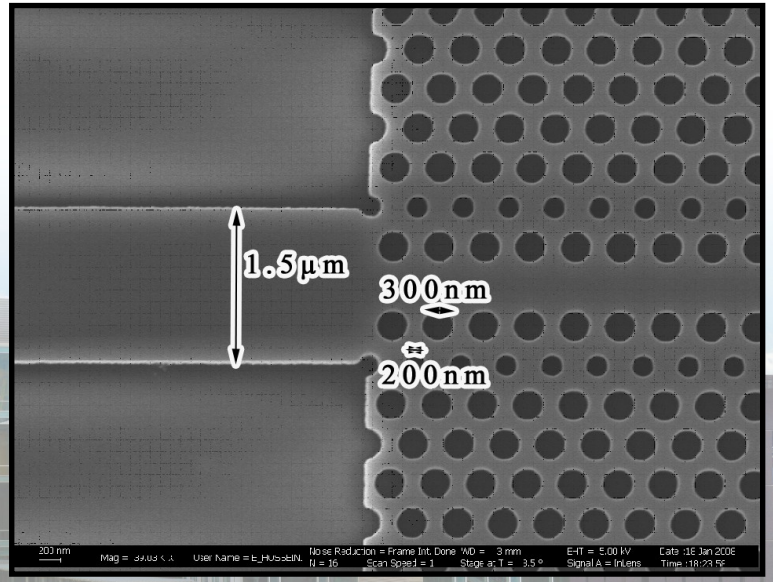
- Micro-turbines
- MEMS gyroscopes
- MEMS accelerometers

Cl_2 based Si etch, right images:

- 2D photonic crystals
- Waveguides

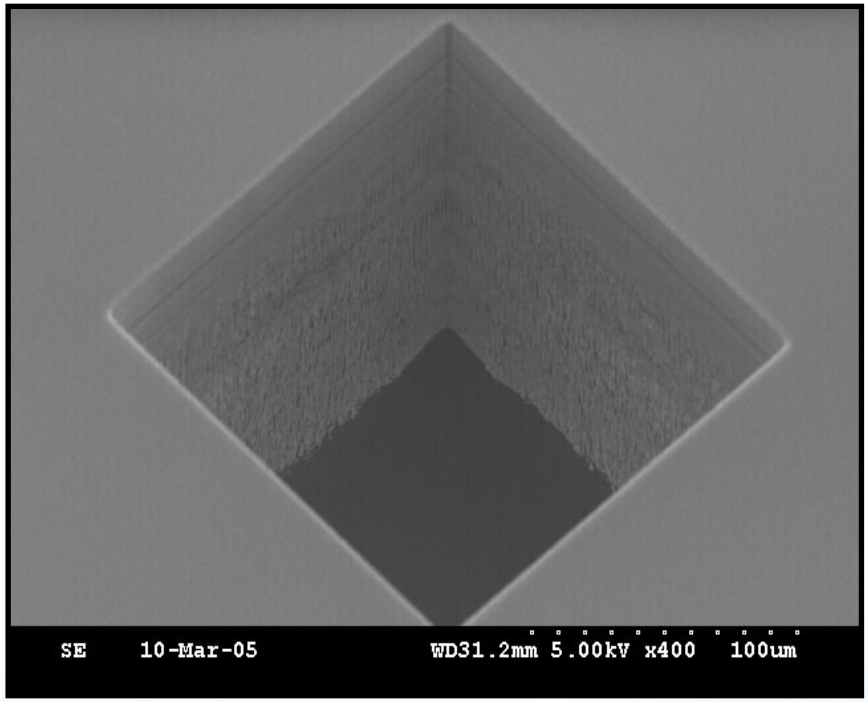


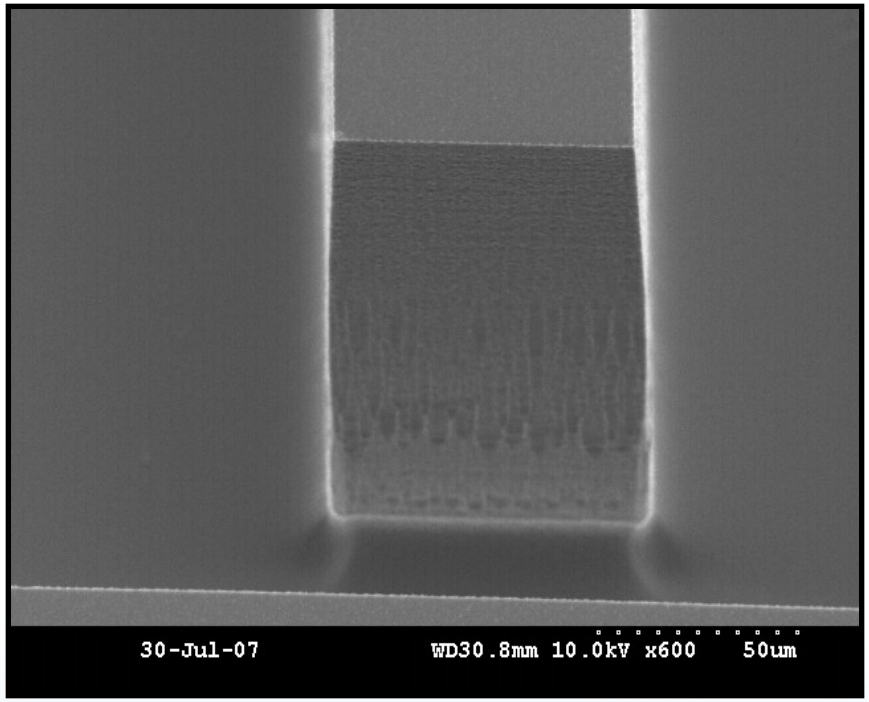




PlasmaTherm DRIE – Si Trench

Images provided by: left, Kianoush Naeli, IEN; right, Chang-Kyeon Ji, PI: Mark Allen





Left image: through-wafer via Applications

- Through-wafer etching
- Deep trench etching for MEMS apps

Right image: cross-section of through-wafer via Rules, Right/Bosch chamber:

- No metal
- Through wafer etching requires carrier

Plasma-Therm SLR RIE (2008)

Pettit Cleanroom

RIE System Featuring:

- Loadlock and load arm

Materials etched and acceptable masks:

- Etched: Al, Cr, Ti, Si; III-V
- Masks: Photoresist; No SU8, BCB

Component specifications (both):

- 500W 13.56MHz RFPP RF-5S power supply

Gases:

- BCl_3, Cl_2, O_2, Ar, H_2

Process Pressure: 5-80mTorr

Substrate: small pieces – one 8” wafer

Temperatures:

- Platen 5-40°C

Plasma-Therm RIE (1986)

Pettit Cleanroom

Dual Chamber Etching System Featuring:

- Si, SiO_2, Si_3N_4 & Al / metal etching
- III-V etching
- Polymer etching

Materials etched and acceptable masks:

- Left: Al, Cr, Ti, Si, poly-Si, metals, III-V
- Right: Si, SiO_2, Si_xN_y polyimide, SU8. BCB
- Masks: Metal and PR

Component specifications (both):

- 500W 13.56MHz RFPP RF-5S Power supply

Gases:

- Left: O_2, BCl_3, Cl_2, Ar
- Right: Ar, CHF_3, O_2, CF_4/SF_6

Process pressure: 10-800mTorr both chambers

Substrate:

- Left – small pieces – one 8” wafer
- Right: small pieces - four 100mm wafers

Temperatures:

- Left Platen 40°C; Right 40°C

Advanced Vacuum Vision 1 and 2 (2007)

Pettit Cleanroom (1) & Marcus Cleanroom (2)

Materials etched and acceptable masks:

- Etched: SiO_2, Si_3N_4, Si
- Masks: metals and photoresist

Component specifications:

- 600W 13.56MHz Seren power supply

Gases:

- Ar, N_2, O_2, CF_4, SF_6, H_2

Process Pressure: 10-800mTorr

Substrate: Small pieces – one 8” wafer

Temperature: 5-40°C

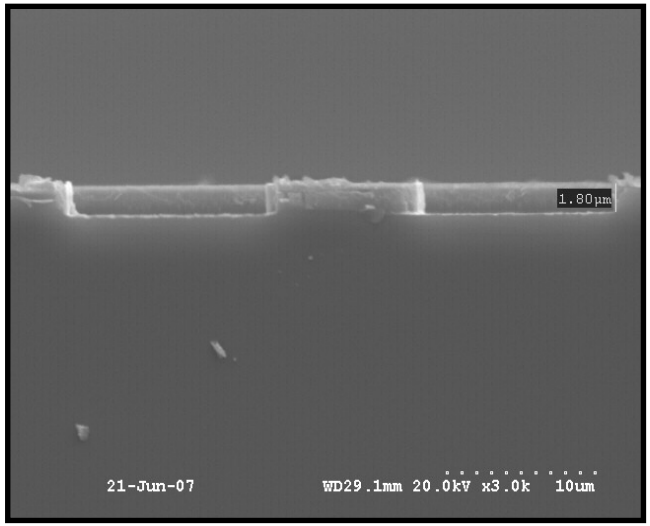
Recent Service/Modification:

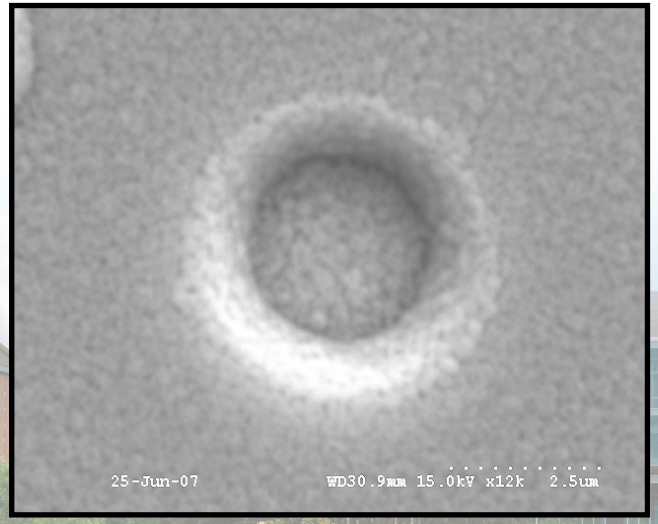
- Vision 2 moved to Marcus Cleanroom
- Full electrode rebuild for both units
- Hoist rebuild for Vision 2
- Power supply service both units

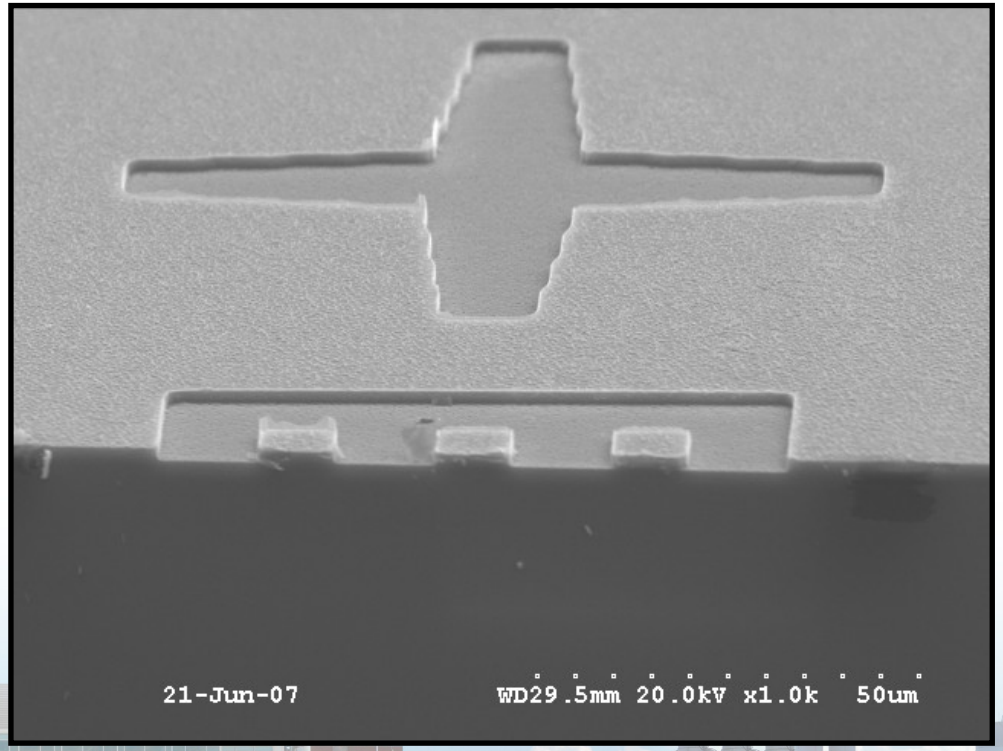
Georgia Tech Institute for Electronics and Nanotechnology

Advanced Vacuum Vision RIE Examples

Lower left image provided by Jamie Zahorian. PI: Levent Degertekin, GT Dept of Mechanical Engineering. Upper left and upper right images provided by Christina Scelsi, MiRC.







Oxford End-Point RIE

Marcus Cleanroom

Functions:

- General plasma etching
- EPD not currently installed

Materials etched and acceptable masks:

- Etched: SiO_2, Si_yN_x
- Masks: photoresist, metal

Component specifications:

- 500W 13.56MHz AE – Platen
- Power: 300W

Gases: Ar, O_2, CHF_3, CF_4

Process Pressure: 5-500 mTorr

Substrate: small pieces – one 4” wafer

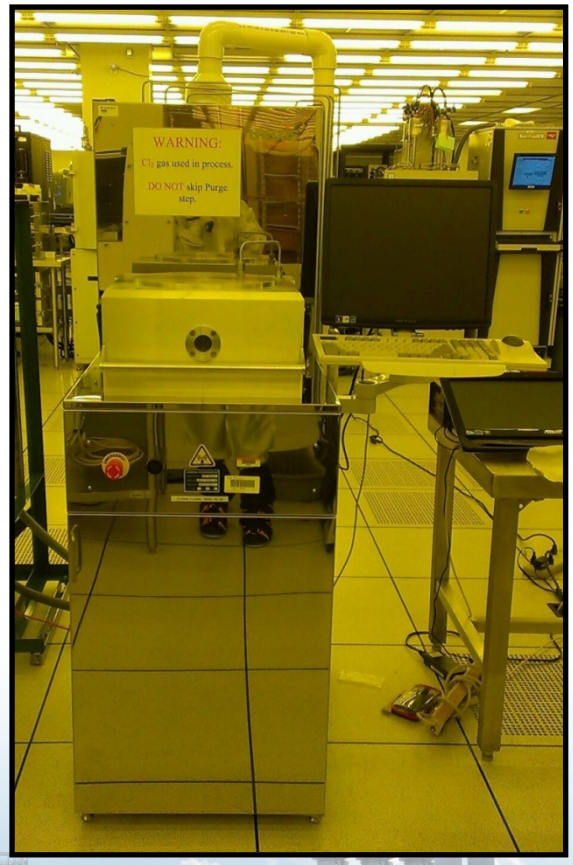
Temperatures: 5-45˚C

Issues:

- Intermittent I/O failures. Possible candidate for PLC/CtrLayer Upgrade

Unaxis RIE

Marcus Cleanroom



Functions:

- Shallow silicon etching

Materials Etched and acceptable masks:

- Si
- Masks: Si_3N_4, SiO_2, photoresist

Component specifications:

- 500W 13.56MHz AE RF5S– Platen

Gases: Cl_2, BCl_3, O_2, Ar

Process Pressure: 10-800mTorr

Substrate: small pieces-4” wafer (up to 3)

Temperatures: 5-40°C

Issues

- GFI fails, had to bring in external 120vac

Georgia Tech Institute for Electronics and Nanotechnology

STS HRM ICP

Marcus Cleanroom

Functions:

- MEMS-CMOS processes
- Narrow high aspect-ratio trench etching

Materials etched:

- Etched: Si, SOI wafers

Masks:

- SiO_2, Si_xN_y
- Photoresists: SC1800 series, SPR220 from Shipley, AZ4000 series from Clariant, NPR from Futurex

Component specifications:

- Coil: 3000W 13.56MHz AEI
- Platen HF: 500W 13.56MHz ENI
- Platen LF: 500W 380KHz AEI LF5
- HBC w/ ESC

Gases: SF_6, C_4F_8, Ar, O_2, CO_2

Process Pressure: 5-80mTorr

Substrate: small pieces (with carrier wafer) - 6” wafers

Temperatures: -20˚C-100˚C

Recent Service/Modification:

- Attempted backup of HDD, always fails, slipstream needed to recover.
- Wafer mapping failures. Resolved by replacing IR wafer detector.
- Intermittent failures of interlock chain. Resolved by replacing soldered relay on I/O board.
- Power supply serviced. Spare purchased.

Y.E.S.-R1 Plasma Cleaner

Pettit Cleanroom

Functions:

- Descum and remove residual organics and thin oxides
- Controlled through MicroLogix PLC upgrade

Component specifications:

Gases: O_2 , Ar, N_2

Process Pressure: 1500mTorr

Substrate: size varies upon user request

Temperatures: 25-80˚C

Gasonics Asher

Marcus Cleanroom

Functions:

- Photoresist stripper for front and backsides of wafers
- Descum (200-500 Angstroms of photoresist)
- Remove max 1 micron each run

Component specifications:

- Load arm

Gases: O_2 and N_2

Process Pressure:

Substrate: 4” wafers, 1-10 wafers per run

Temperatures: 25-200°C

Xactix XeF_2 e1 Series Xetch (2008)

Marcus Cleanroom

Vendor-specified system features:

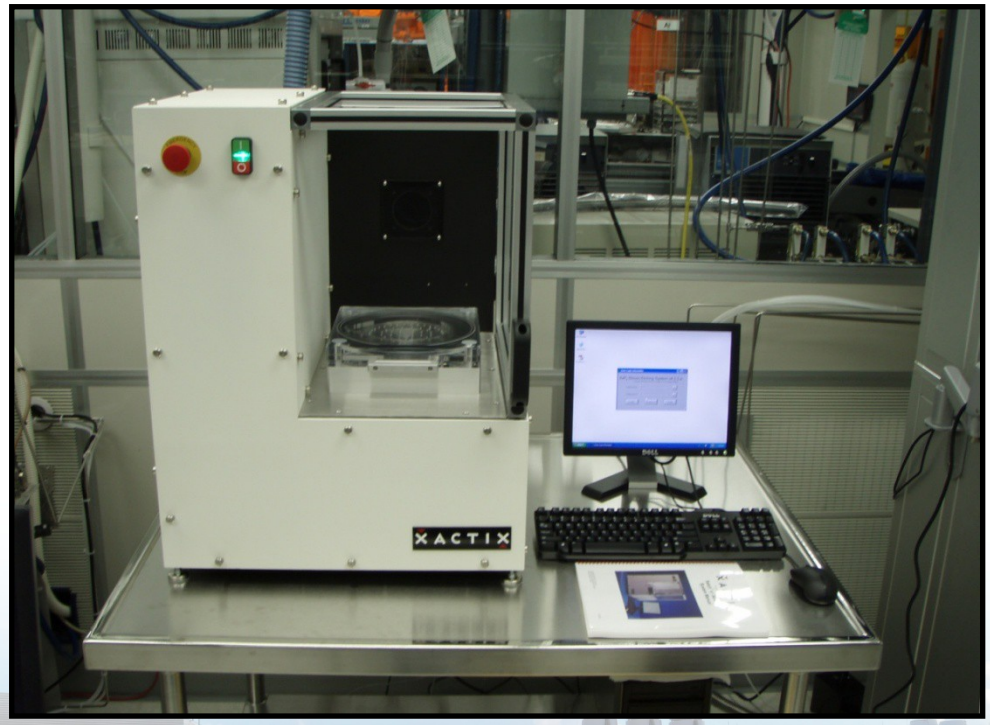
- Excellent selectivity SiO_2:Si (1000:1), good selectivity to PR
- Potential to etch very small devices (30nm)
- Etch does not attack Bosch passivation layer – can switch between tools and still protect trench walls

Materials etched and acceptable masks:

- Etched: Si, poly-Si
- Masks: PR, SiO_2, Si_3N_4

Gases: XeF_2

Substrate: 1 die - 150mm wafer (specialized chuck)



Georgia Tech Institute for Electronics and Nanotechnology

Technics Micro-RIE 1&2

Instructional Center and Soft Lithography Suite

Functions:

- Simple descum and surface activation
- Low entry cost

Materials etched:

- Etched: Si, polymer

Gases: O2, N2

Substrate: small pieces - 100mm wafer

LFE Barrel Etcher

Soft Lithography Suite

Functions:

- Simple descum and surface activation
- High pressure: 1 - 5 Torr
- Low entry cost

Materials etched:

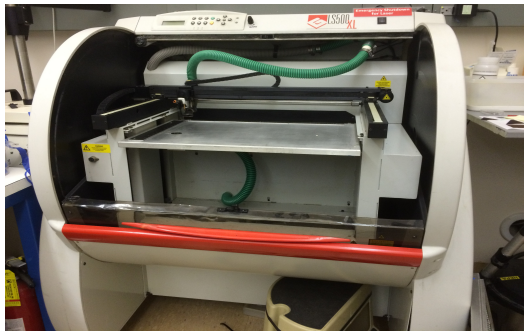
- Etched: Si, polymer

Gases: O2, Air

Substrate: small pieces - 100mm wafer

Lasers
Pettit Laser Lab

Hermes LS500XL CO2



Functions:

- CO2 laser @60W, approx 1mm wavelength
- Resolutions of 200um spot and sub mm movement

Materials etched:

- Polymers, wood, papers, plastics, angstrom thin metals

Resonetics IR

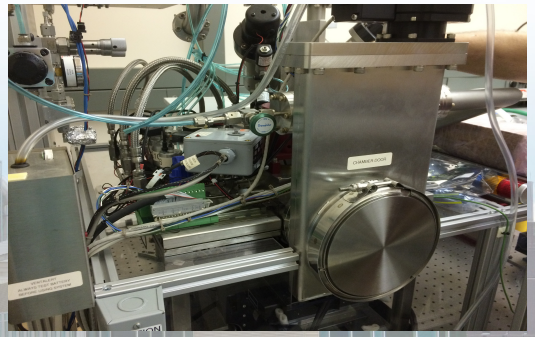
Functions:

- Nd-YLF laser @16W, 1047nm wavelength, 20us pulse/ms
- Resolutions of 50um spot and sub um movement

Materials etched:

- Any metal up to 200um thick

TeraVision LCE (Down)



Functions:

- Freq. Doubled 532nm laser
- Cl2 environment, heated chamber to just below Cl2 activation, activated by laser.
- Resolutions of 2um, 1um depth/pass

Materials etched:

- Si

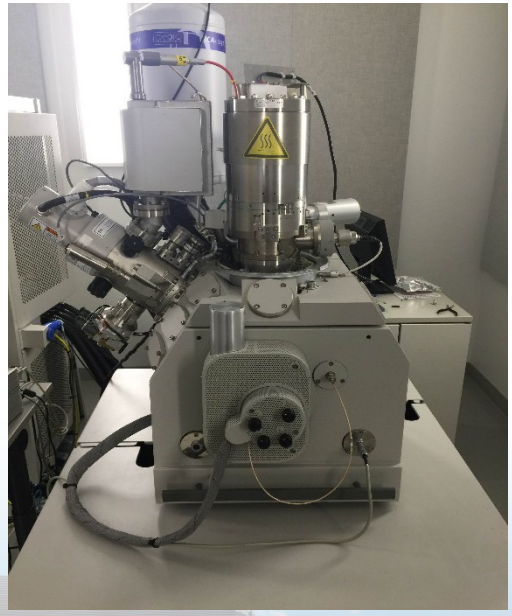
Georgia Tech Institute for Electronics and Nanotechnology

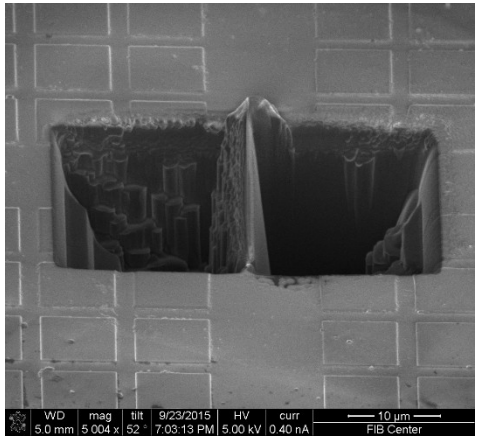
FEI Nova Nanolab 200 FIB/SEM

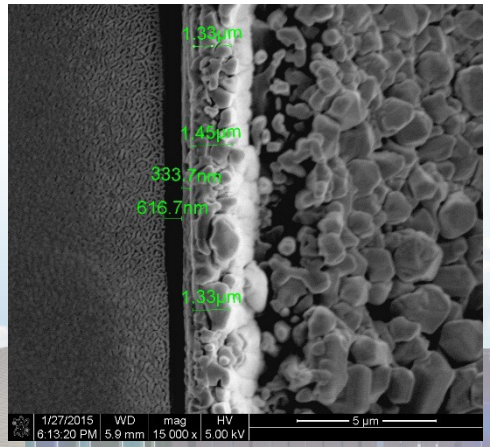
Marcus Microscopy Center

Vendor-specified system features:

- Ga ion beam, 30nm min. line width etched
- 40nm Pt line deposition
- TEM lamella preparation via micro-manipulator
- EDX of cross-sections
- Circuit editing via etching and deposition of Pt







Georgia Tech Institute for Electronics and Nanotechnology

JEOL JBX-9300FS E-Beam Lithography

Pettit Cleanroom

:: Introduction ::

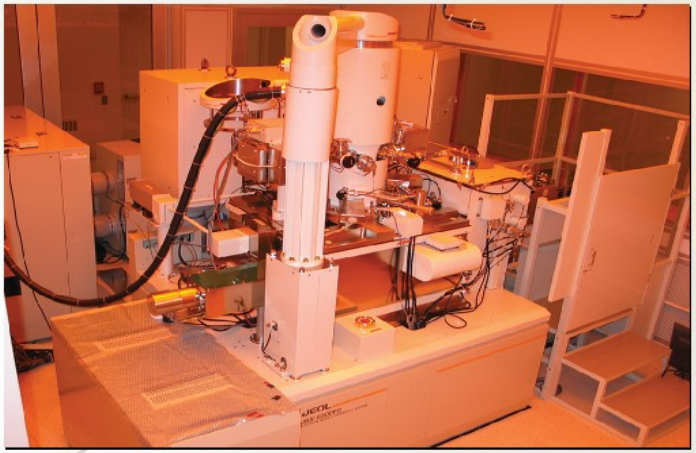
The IEN currently operates a JEOL JBX-9300FS 100kV electron beam lithography system. The JBX-9300FS features a spot beam, vector scan, a step and repeat stage, and is capable of varying the beam size widely. Its dynamic correction system eliminates defocusing resulting from beam deflection.

:: Technical Characteristics ::

- 4nm diameter Gaussian spot electron beam
- 50kV/100kV accelerating voltage
- 50pA – 100nA current range
- 50MHz scan speed
- +/- 100um vertical range automatic focus
- +/- 2mm vertical range manual focus
- ZrO/W thermal field emission source
- vector scan for beam deflection
- max 300mm (12") wafers with 9" of writing area
- < 20nm line width writing at 100kV
- < 20nm field stitching accuracy at 100kV
- < 25nm overlay accuracy at 100kV

Available Cassettes:

- Wafer
  - 75mm, 100mm, 150mm, 200mm diameter
  - 300mm can be purchased for up to 9" square writing area
- Masks
  - 5" mask, 6" mask
- Pieces
  - minimum 3 x 5mm piece
- 5" and 6" square mask loading



Trainer: Devin Brown, *Senior Research Engineer*
404.385.4220
devin.brown@mirc.gatech.edu
Location: Pettit Cleanroom

Why E-Beam Lithography?

- Exceeds patterning capability of optical lithography
  - Easily pattern sub-micron features
  - IEN has demonstrated 6.5nm features
- Patterns rapidly created from CAD file
  - No mask necessary as in optical lithography
  - Rapid turn-around on design modifications, ideal for research

Georgia Tech Institute for Electronics and Nanotechnology

Contact Information

If you have any questions, concerns or service requests, please contact us at plasmateam@ien.gatech.edu